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INSTRUCTION MANUAL
MODEL 600F
DATA TRANSMISSION
TEST SET

JULY 1972

REVISION

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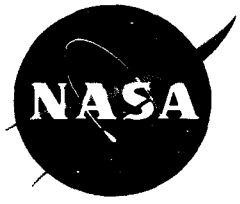

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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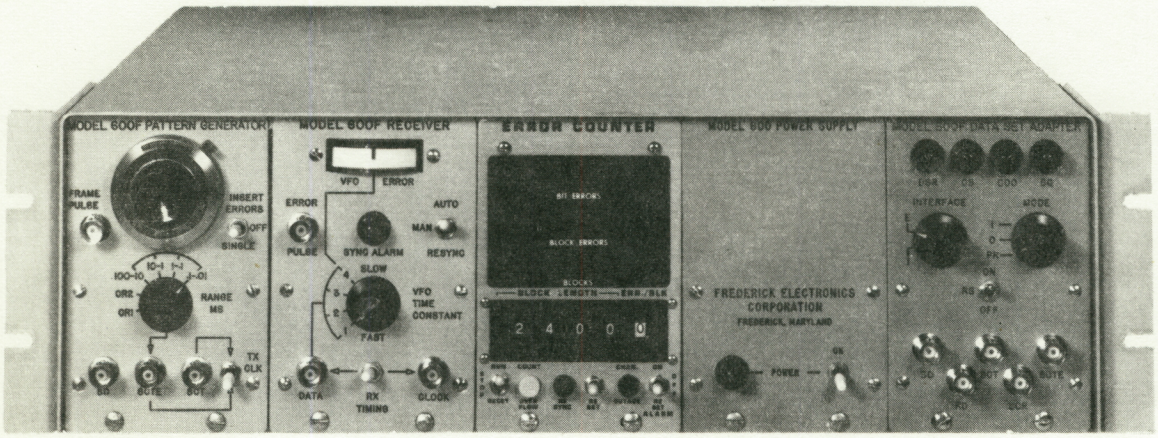


Figure 1-1. Model 600F Data Transmission Test Set

B

SECTION 1

INTRODUCTION

1.1 SCOPE AND PURPOSE OF MANUAL

This manual provides information necessary for the operation and maintenance of the Model 600F Data Transmission Test Set. The manual contains a description of the physical and functional characteristics; pertinent installation data; instructions for operating the equipment; general and detailed principles of operation; preventive and corrective maintenance procedures; and block, logic, and component layout diagrams of the equipment and its major component assemblies.

1.2 GENERAL DESCRIPTION

The Model 600F Data Transmission Test Set is designed specifically for testing data transmission systems by means of error counting techniques. The Model 600F comprises the following five modules: the pattern generator, the receiver, the error counter, the power supply, and the data set adapter. The pattern generator is the source of data for transmission over the system being tested. The receiver receives incoming test data from data sets (modems), establishes and maintains bit and pattern synchronization, recognizes pattern errors, and develops error pulses for readout by the error counter module and for external equipment. The error counter module counts the number of errors in the incoming data, defines and counts block errors, and provides a visual display of bit errors, block errors, and total blocks received. In addition, it provides resync commands to the receiver during specified modes of operation and error rate conditions. (A compatible error counter module, the Model 600, with a mechanical totalizer for bit errors, and employing a different resync technique, is used in some units. Characteristics of the Model 600 error counter are given in Appendix B of this manual.) The data set adapter serves as a signal level converter between the Model 600F internal signal levels and data sets and provides conditioning and display of the status of other data set interface control signals. The power supply provides operating voltages for the Model 600F.

The Model 600F is most commonly applied to performance measurement situations in which the system units to be tested are in different locations. As a result, two units are required - one at each end of the system. In this application, each Model 600F serves to transmit the test

pattern to the remote unit and, simultaneously, to receive the test pattern from the remote unit and perform the test measurement, thereby testing both ends of a full duplex transmission system. A single Model 600F can also be used to perform simultaneous transmission and reception of test data on data sets connected back-to-back.

1.2.1 PHYSICAL DESCRIPTION

The Model 600F contains five plug-in modules, each 3-3/8 inches wide by 5-1/8 inches high. The modules are collectively housed in an all-metal cabinet which is 5-1/4 inches high by 19 inches wide by 18 inches deep. The complete unit can be mounted in a standard 19-inch relay rack. The total weight of the unit is approximately 30 pounds. The unit is shown in Figure 1-1.

All electronic circuits for each module are solid-state components, packaged in the form of plug-in printed circuit boards. Table 1-1 contains a complete list of the boards in each module. Board layout emphasizes the segregation of functions into logical units to allow easy trouble isolation. To facilitate maintenance and testing, an extender cable and extender boards are supplied. These items permit defective modules to be removed from the cabinet for power-on trouble-shooting and circuit analysis. Frequently used operating controls, indicators, and connectors are located on the front panel of the Model 600F. In addition, the following items are available on the rear panel of the Model 600F: (1) Two terminal strips for an external printer, (2) a Cannon connector, and (3) an ac line cord.

1.2.2 FUNCTIONAL DESCRIPTION

Figure 1-2 is a simplified block diagram of the Model 600F. The pattern generator provides a pseudorandom data pattern which repeats every 2047 bits. The pattern bit rate is timed from either an internal (SCTE) source located in the pattern generator module or an external (SCT) drive source, as selected by a front-panel switch. When the internal (SCTE) source is selected, timing is provided by a variable frequency oscillator (VFO) or by one of two crystal-controlled oscillators. The generated pattern is routed through the data set interface for level conversion and then transmitted to the data set. Clock signals from the internal source are also routed through the data set interface and transmitted to the data set.

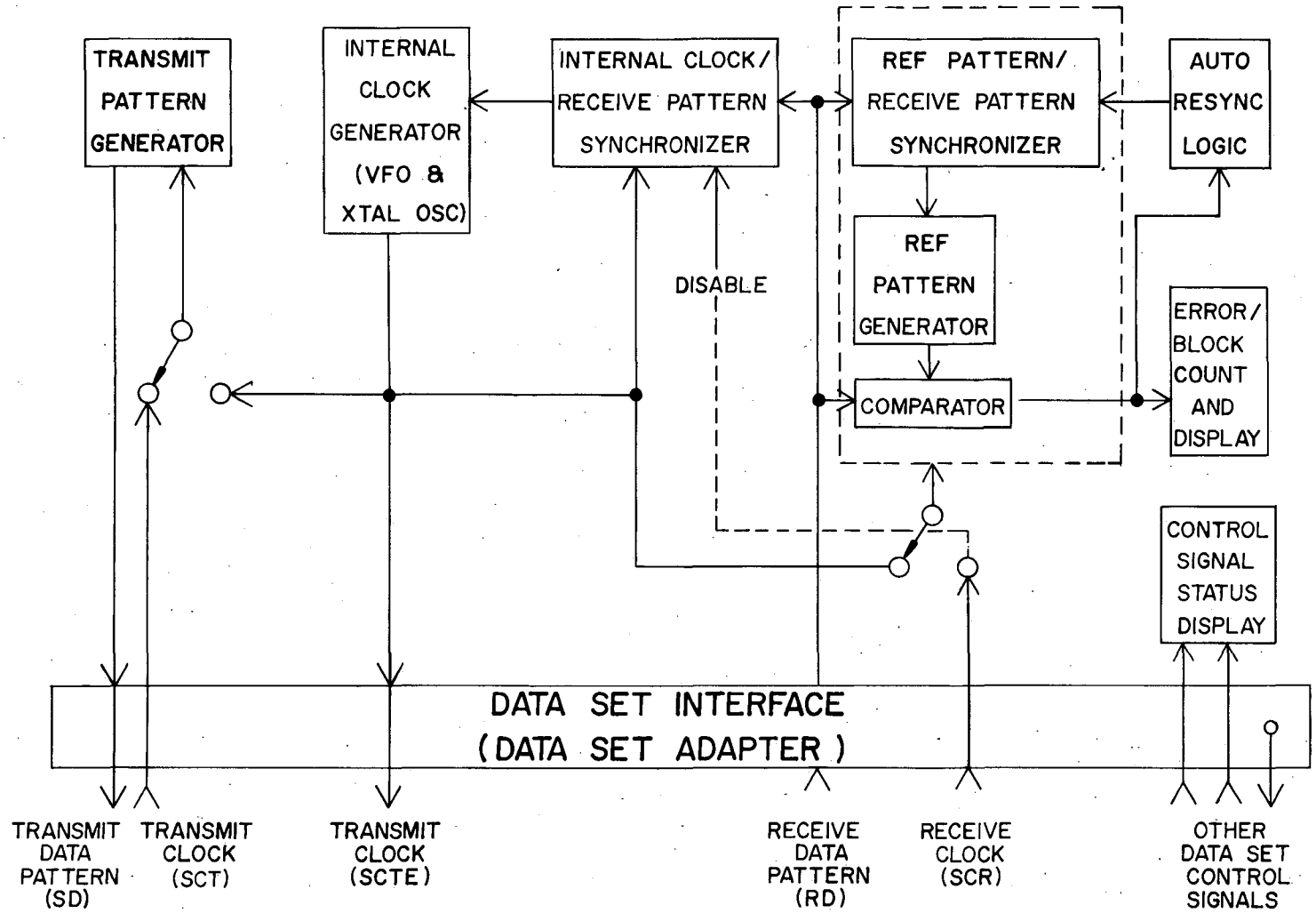


Figure 1-2. Simplified Block Diagram

Receive test data from the data set is conditioned in the data set interface, and then is applied to the reference pattern/receive pattern synchronizer and to the error comparator, located in the receiver module, where it is compared bit-by-bit with the internally generated reference pattern. Any disagreement between the pattern produces an error pulse which is routed into the error counter module. The internally generated reference pattern is synchronized with the incoming data by synchronizer circuits located in the receiver module. Synchronization is initiated either manually by means of a front-panel switch or automatically by a command pulse from the error counter module.

The reference pattern bit rate is timed from either the internal clock source located in the pattern generator module, or from an external clock source (SCR), as selected by a front-panel switch. When timing is obtained from the internal clock source, its frequency is set to the same frequency as the incoming data by means of front-panel controls on the pattern generator module. A form of automatic frequency control, derived from the incoming data by circuits in the receiver module, corrects the VFO or the crystal oscillator so that it is always in proper phase relationship with the incoming data.

Visual display of bit errors, block errors and blocks counted, together with an indication of system quality are provided by the error counter module. Logic circuits in the error counter module monitor the incoming data patterns and during specified modes of operation and error rate conditions, issue a command signal which initiates resynchronization in the receiver module.

The data set interface contains level converters for interface between the Model 600F and data sets. Circuits are also provided to condition the data set control and status signals to drive front-panel display lamps.

1.3 EQUIPMENT CHARACTERISTICS

The physical and electrical characteristics of the Model 600F are provided in Table 1-2.

1.4 FUSE COMPLEMENT

A 1/2-ampere Slo-Blo fuse, designated A5F1, is used in the power supply module. This fuse is located inside the module, below and to the rear of the chassis. A 1-ampere fuse, designated A4F701, is used in

the error counter module power supply. This fuse is located on the lower left corner of the chassis rear bracket.

1.5 EQUIPMENT REQUIRED

1.5.1 EQUIPMENT SUPPLIED

A complete list of the Model 600F equipment is shown in Table 1-3.

1.5.2 TEST EQUIPMENT

Test equipment required for check-out and maintenance of the Model 600F is described in Section 5.

Table 1-1

MODEL 600F PRINTED CIRCUIT BOARDS

Module	Boards Per Module	Board Ref. Number	Description
Pattern Generator	4	NO345	Shift Register Generator
		NO346	Dividers
		NO347	VFO and Dividers
		NO348	Crystal Oscillator and Divider
Receiver	2	N39079	Synchronizer and Error Detector
		NO350	Input and Phase-Lock
Error Counter	8	064-152-000-4	Recognizer
		064-156-000-4	Outage Indicator
		064-148-000-4	Counter Display Control
		064-154-000-4	Translator
		064-135-000-4	Counter Display (3 Boards)
		064-144-000-4	Power Supply

Table 1-1

MODEL 600F PRINTED CIRCUIT BOARDS (Cont)

Module	Boards Per Module	Board Ref. Number	Description
Power Supply	No Boards		
Data Set Adapter	2	NO330	Level Converters
	1	NO355	Mother Board

Table 1-2

EQUIPMENT CHARACTERISTICS

Characteristic	Value
Dimensions	
Height	5.25 in.
Width	19 in.
Depth	19.5 in.
Weight	30 lbs (approx)
Power Requirements	115 vac, 47 to 63 Hz single-phase, 64 watts approx
Input Levels	Mode E: -6 volts minimum for logical "1" +6 volts minimum for logical "0" Mode I: More than 23 ma for logical "1" less than 5 ma for logical "0"
Input Impedance	Mode E: 5000 ohms (nominal) Mode I: 100 ohms
Output Levels	Mode E: Into 1000 ohm load: +6 volts minimum for space or logical "0"; -6 volts minimum for mark or logical "1"

Table 1-2

EQUIPMENT CHARACTERISTICS (Cont)

Characteristic	Value
Output Levels (Cont)	Mode I: Into 100 ohm load: greater than 23 ma for space or logical "0"; less than 5 ma for mark or logical "1"
Send Signal Rise and Fall Time	Mode E: 6 microseconds (approx) Mode I: 1 microsecond (approx)
Data Output	PR Mode: Pseudorandom pattern with 2047 bit period 0 Mode: A steady logic "0" 1 Mode: A steady logic "1"
Pulse Rates	10 to 100,000 bps with internal variable frequency oscillator; two preselected rates between 300 and 7200 bps with internal crystal oscillators; 10 to 150,000 bps with external timing
Time Constant Range of Automatic Frequency Control	10 milliseconds to 10 seconds
Raw Error Pulse (TB1)	+10 to -10 volts, 1/2 bit length
Controlled Error Pulse (TB2)	0 to -10 volts, 1/2 bit length
Mode of Operation	Full duplex, clocked from an internal or an external timing source
Model 1225 Error Counter Module	
Block Length Counter	0001 through 9999 bits per block

Table 1-2

EQUIPMENT CHARACTERISTICS (Cont)

Characteristic	Value
Model 1225 Error Counter Module (Cont)	
Number or Errors per Block Threshold	0 through 9
Maximum Count of BIT ERRORS Displayed	999, 999
Maximum Count of BLOCK ERRORS Displayed	999, 999
Maximum Count of BLOCKS Displayed	999, 999
Resync Criteria (Resync between internal reference pattern and data pattern received from data set)	Probability of Resync when true loss of sync has occurred = 0.99 or higher for: a. 100 bit times when received bit error probability is 0.00 b. 2000 bit times when received bit error probability is greater than 0.00 and is equal to or less than 0.25
False Resync Probability	Probability of Resync when, in fact, the Model 600F has not lost sync = 0.01 or less for: a. 9×10^9 bit times when received pattern has bit error probabilities in the range of 0.00 to 0.25 b. 9×10^9 bit times when received data is a fixed pattern of all "0", all "1", or repeated "1000" c. One error burst in the received data. (A "burst" is a series of up to 2000 bits with probability of error between

Table 1-2

EQUIPMENT CHARACTERISTICS (Cont)

Characteristic	Value
False Resync Probability	0.25 and 0.5 preceded and succeeded by data bits with error probability of error between 0.00 and 0.25) d. 10^6 bit times when received data has bit error probabilities in the range of 0.25 to 0.50

Table 1-3

MODEL 600F EQUIPMENT LIST

Item	Reference Symbol	Quantity
Pattern Generator Module	A2	1
Receiver Module	A3	1
Error Counter Module	A4	1
Power Supply Module	A5	1
Data Set Adapter Module	A6	1
Extender Board	A8	2
Extender Cable	A7	1
Adapter Cable	A9	1
Equipment Cabinet	A1	1

SECTION 2

INSTALLATION

2.1 INTRODUCTION

This section provides instructions concerning installation of the Model 600F Data Transmission Test Set and checkout procedures to be performed to ensure that the equipment is ready for normal operation.

2.2 INSTALLATION PLANNING

Since the Model 600F is used for testing data transmission systems, it is desirable that the unit be physically located near the terminals and controls of the system under test. The unit should be installed in a standard 19-inch equipment rack equipped with a 115-volt 50/60 Hz power outlet with a grounding contact and with power handling capacity of at least 100 watts.

2.3 INSTALLATION PROCEDURES

2.3.1 UNPACKING

Carefully unpack and remove the Model 600F from its shipping container and inspect the unit for damage. If any damage is found, file a claim with the shipping agency.

2.3.2 MOUNTING

Mount the Model 600F in a standard 19-inch equipment rack. A vertical rack space of 5-1/4 inches is required. Secure the unit to the rack by means of four screws. Connect the unit power cord to a 115-volt 50/60 Hz power outlet and set the POWER ON switch to the ON position. The low power consumption of the unit permits operation over a temperature of 0° to 50° C.

2.3.3 POWER REQUIREMENTS

Each Model 600F is shipped ready to operate from a power source of 115 volts ac, 60 cycles-per-second, single phase. Total power consumption is approximately 64 watts. Satisfactory operation is possible with frequencies from 47 to 63 cycles-per-second.

CAUTION

Although the Model 600F power supply module is also wired to operate from a 240-vac power source, under no circumstances may a Model 600F equipped with a Model 1225 error counter module be operated on 240 vac. If attempted, severe damage to the error counter module will result.

2.3.4 INTERCONNECTIONS

Interconnections between the Model 600F and the system under test are provided by a 25-pin Cinch connector (J7) located on the rear chassis (see Figure 2-1). Pin allocations are listed in Table 2-1. Unlisted pins are not used. Normally, the front panel BNC connectors on the data set adapter module are used only for monitoring data and timing signals to and from the rear connector; however, where it is more convenient, system connections can be made directly to these BNC connectors. (Note that the cable must be removed from J7 before making these connections.) Those front panel BNC connectors that are connected directly to a rear connector pin are also listed in Table 2-1.

In addition to J7, two rear panel terminal strips (TB1 and TB2) provide auxiliary outputs. Table 2-2 describes the function of each connection on the terminal boards. Terminal board TB1 provides frame ground, bipolar error pulses, and duplicate clock pulses used in timing the reference pattern generator in the receiver module and the logic circuits in the error counter module. Terminal board TB2 provides negative 12-volt logical "one" outputs for resync, channel outage, block count, block error, and bit error pulses. Auxiliary outputs are provided for an external printer or counter. Typical installation connections for the Model 600F are shown in Figure 2-2.

2.4 CHECKOUT AND ADJUSTMENT

2.4.1 GENERAL

The checkout and adjustment procedures described in the following paragraphs should be performed prior to placing the Model 600F in operation in order to obtain optimum performance from the unit. Test equipment required for checkout and adjustment are an oscilloscope

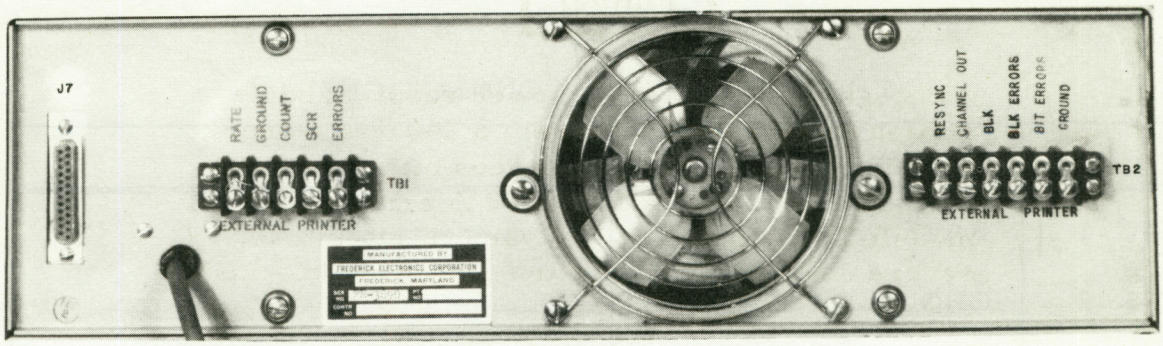


Figure 2-1. Rear Panel Connectors

Table 2-1

INTERFACE CONNECTOR (J7) PIN DESIGNATIONS

Pin	Designation	Associated BNC Connector
1	Frame Ground - FG	
2	Send Data - SD	SD (Data set adapter TP5)
3	Receive Data - RD	RD (Data set adapter TP4)
4	Request to Send - RS	
5	Clear to Send - CS	
6	Data Set Ready - DSR	
7	Signal Ground - SG	
8	Carrier On-Off - COO	
15	Serial Clock Transmit - SCT	SCT (Data set adapter TP2)
17	Serial Clock Receive - SCR	SCR (TP3)
21	Signal Quality - SQ	
24	Serial Clock Transmit External - SCTE	SCTE (TP1)

Table 2-2

TERMINAL BOARD CONNECTIONS

Pin	Designation	Function
TB1-1	RATE	No connection
-2	GROUND	Common ground
-3	COUNT	Not used with the Model 1225 error counter module. (Error count output from Model 600 error counter module to external printer)
-4	CLOCK	Clock signal selected by RX TIMING switch
-5	ERRORS	Receiver bit error pulses
TB2-1	RESYNC	Pulse indicating receiver resynchronization is in process (defined by Model 1225 error counter module)
-2	CHANNEL OUT	Signal which indicates that error rate over ten second period has exceeded 25 percent
-3	BLK	Block count pulses (received clock divided by block length selected by Model 1225)
-4	BLK ERRORS	Block error pulses (blocks meeting block error criterion selected by Model 1225)
-5	BIT ERRORS	Received bit errors controlled by AUTO INHIBIT-CONT switch on the counter display control board of the Model 1225
-6	GROUND	Common ground

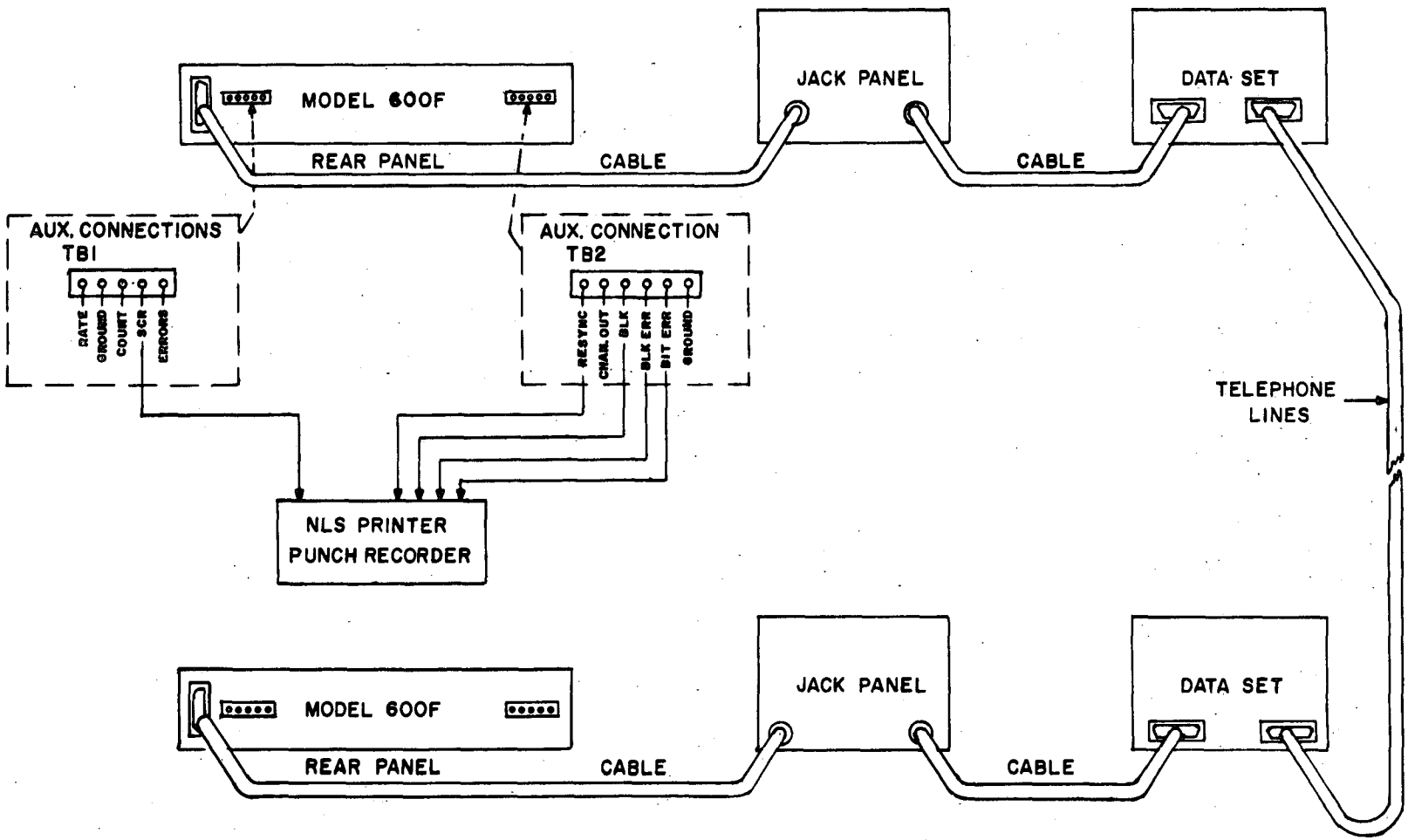


Figure 2-2. Model 600F, Typical Installation Connections

(Tektronix 535A or equivalent), an electronic frequency counter (ATEC 6C46 or equivalent), and a squarewave generator. Prior to performing the following proceedures, set the Model 600F on a workbench where modules to be adjusted will be supported while connected to the extender cable. Connect the unit power cord to a 115-vac outlet and set the POWER ON switch to the ON position.

2.4.2 SIGNAL LEVEL MEASUREMENTS

To make the signal level measurements, proceed as follows:

a. On pattern generator module front panel, set SCTE-SCT switch, S1, to SCTE position. On data set adapter front panel, set INTERFACE switch, S3, to I position.

b. On pattern generator front panel, set RANGE MS switch to .1-.01 position and vernier dial to 1.00 position. These settings adjust SCTE bit rate to 100 kbs.

c. On data set adapter front panel, connect a cable between SCTE BNC connector and RD BNC connector using a "T" connector on SCTE BNC.

d. Connect oscilloscope to SCTE BNC "T" connector and observe 0- to 5-volt peak-to-peak squarewave with cycle period of approximately 0.01 millisecond. This checks operation of VFO in pattern generator module and SCTE level converter in data set adapter module.

e. Connect oscilloscope to DATA BNC connector on receiver module and observe 0- to negative 10-volt peak-to-peak squarewave with same cycle period as in step d. This checks operation of RD level converter in data set adapter.

f. Disconnect cable from RD BNC connector and connect to SCR BNC connector on data set adapter, and connect oscilloscope to CLOCK BNC connector on receiver module. Observe squarewave as in step e. This checks operation of SCR level converter in data set adapter.

g. Disconnect cable from SCR BNC and connect to SCT BNC on data set adapter, and connect oscilloscope to

SCT BNC connector on pattern generator module. Observe squarewave as in step e. This checks operation of SCT level converter in data set adapter.

h. Connect a cable between SD BNC connector and RD BNC connector on data set adapter front panel using a "T" connector on SD BNC.

i. Connect oscilloscope to SD BNC "T" connector and observe 0- to 5-volt peak-to-peak pseudorandom pattern with bit length of approximately 0.01 millisecond. This checks operation of shift register in pattern generator module and SD level converter in data set adapter.

j. With oscilloscope still connected to SD BNC "T" connector, set MODE switch to 0 position and observe a steady 5-volt level; set MODE switch to 1 position and observe a steady 0-volt level.

k. Set RANGE MS switch to 1-.1 position to adjust SCTE bit rate to 10 kbs, and repeat steps c through j with MODE switch set to E position. The waveforms observed in steps d and i should have a peak-to-peak value of -8 volts to +9 volts. The levels observed in step j should be a steady positive 9-volts in the 0 position, and a steady negative 8-volts in the 1 position.

2.4.3 DATA SET ADAPTER LAMP DRIVERS

a. Locate pin 4 of rear mounted connector J7 (see Figure 6-19). This pin connects to pole of RS switch S2 on data set adapter front panel.

b. Measure voltage between pin 4 of J7 and chassis ground when RS switch is set to ON and OFF positions. Voltage should be +12 volts in ON position, and -12 volts in OFF position.

c. Connect jumper wire between following pins, two pins at a time: from pin 4 to pin 6 (DSR), pin 4 to pin 5 (CS), pin 4 to pin 8 (COO), and pin 4 to pin 21 (SQ). While each connection is made, set RS switch to ON and OFF positions. Corresponding indicator lamp on data set

adapter front panel should glow when RS switch is set to ON position and should extinguish when switch is set to OFF position.

2.4.4 VFO AND VFO PHASE-LOCK ALIGNMENT

Perform the VFO and VFO phase-lock alignment in accordance with the procedures given in paragraphs 5.4.1 and 5.4.2.

2.4.5 CRYSTAL OSCILLATOR ADJUSTMENT

Adjust frequency of crystal oscillators corresponding to RANGE MS switch positions CR1 and CR2 in accordance with the procedure given in paragraph 5.4.3.

2.4.6 OVERALL PERFORMANCE BENCH TEST

The Model 600F should be given an overall performance test to ensure that the unit is operating properly. Perform this test as given in paragraph 5.4.6.

SECTION 3

OPERATION

3.1 INTRODUCTION

This section provides the instructions necessary to turn on, operate, and turn off the Model 600F Data Transmission Test Set. This section also describes front panel controls, indicators, and connectors on the equipment.

3.2 CONTROLS, INDICATORS, AND CONNECTORS

Figure 3-1 and Tables 3-1 through 3-5 identify and describe front panel controls, indicators, and connectors. Control, indicator, and connector names presented with initial capital letters are functional names assigned in the absence of names placarded on the equipment. Names presented in upper case letters are those placarded on the equipment.

3.3 OPERATING PROCEDURES

The following paragraphs provide the operating procedures required for turn-on, operation, and turn-off of the Model 600F.

3.3.1 TURN-ON

To turn on the Model 600F, proceed as follows:

a. Ensure that all required signal connections are made and that power cable is connected to 115-vac power outlet.

b. Set POWER switch to ON position and note that POWER indicator lights.

c. Depress ON-OFF-RESET ALARM switch to RESET ALARM and let switch return to OFF position. If audible alarm is desired, set switch to ON position to enable audible alarm circuitry.

d. Depress RUN-STOP-RESET switch to RESET and let switch return to STOP position.

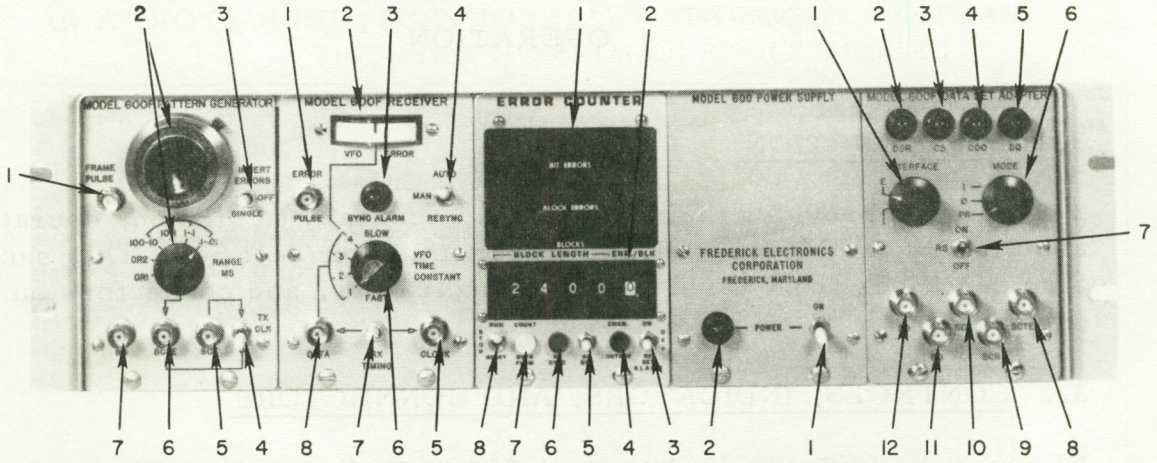


Figure 3-1. Controls, Indicators, and Connectors
(Refer to Tables 3-1 through 3-5)

Table 3-1

PATTERN GENERATOR (A2) CONTROL, INDICATOR, AND DESCRIPTIONS (See Figure 3-1)

Index No.	Name	Type	Function
1	FRAME PULSE (J9)	BNC Connector	Provides negative-going synchronizing pulse, one bit in duration, once per 2047-bit pattern frame
2	RANGE MS (S2)	Rotary Switch	Establishes internal clock range when TX CLK switch is in SCTE position or when RX TIMING switch is in DATA position, as selected by the following switch positions: CR1 — Provides an accurate crystal controlled clock signal with cycle period within the range of 3.33 to 0.139 milli-

Table 3-1

PATTERN GENERATOR (A2) CONTROL, INDICATOR, AND DESCRIPTIONS (Cont) (See Figure 3-1)

Index No.	Name	Type	Function
2 Cont			seconds and bit rate of 300 to 7200 bps, depending on the crystal equipped CR2 — Same function as CR1 position 100-10 — Provides range of 100 to 10 milliseconds and bit rate of 10 to 100 bps 10-1 — Provides range of 10 to 1 milliseconds and bit rate of 100 to 1000 bps 1-.1 — Provides range of 1 to .1 milliseconds and bit rate of 1000 to 10,000 bps .1-.01 — Provides range of .1 to .01 milliseconds and bit rate of 10,000 to 100,000 bps
	Vernier Dial (R1)	Potentiometer	When RANGE MS switch is set for VFO mode operation (any position except CR1 or CR2), provides continuously calibrated adjustment of bit rate within range selected by switch
3	INSERT ERRORS - OFF-SINGLE (S3)	Toggle switch	Provides means of inserting errors in the send data pattern, as selected by the following switch positions:

Table 3-1

PATTERN GENERATOR (A2) CONTROL, INDICATOR, AND DESCRIPTIONS (Cont) (See Figure 3-1)

Index No.	Name	Type	Function
3 Cont			INSERT ERRORS — Causes 1 bit to be generated in error in each 2047-bit frame OFF — Permits normal operation of pattern generator SINGLE (momentary) — Causes single frame error bit per actuation. Error bit is coincident with frame pulse
4	TX CLK (S1)	Toggle switch	In SCT (up) position, selects clock from data set to drive pattern generator In SCTE (down) position, selects internal clock (crystal or VFO) to drive pattern generator
5	SCT (J7)	BNC connector	Provides monitor point for clock signal from data set
6	SCTE (J6)	BNC connector	Provides monitor point for internal clock
7	SD (J5)	BNC connector	Provides monitor point for pseudorandom data output from pattern generator

Table 3-2

RECEIVER (A3) CONTROL, INDICATOR, AND CONNECTOR DESCRIPTIONS (See Figure 3-1)

Index No.	Name	Type	Function
1	ERROR PULSE (J4)	BNC connector	Provides connection for bipolar error pulses from error detector circuits
2	VFO ERROR (M1)	Meter	Provides indication of relative magnitude and direction of VFO error signal to aid in phase-lock of VFO when RX TIMING switch is in DATA position
3	SYNC ALARM (DS1)	Indicator	Lights to indicate that resynchronization is in progress
4	AUTO-MANUAL-RESYNC (S3)	3-position toggle switch	Controls receiver resynchronization in each position, as follows: AUTO — Enables automatic pattern resynchronization when the received data is truly out of sync with the reference data MANUAL — Inhibits automatic pattern resynchronization RESYNC (momentary) — manually initiates resynchronization
5	CLOCK (J6)	BNC connector	Provides front panel monitor point for clock signal from system under test
6	VFO TIME CONSTANT (S1)	Rotary switch	When RX TIMING switch is in DATA position, switch selects VFO phase-lock time constant in each position as follows:

Table 3-2

RECEIVER (A3) CONTROL, INDICATOR, AND CONNECTOR DESCRIPTIONS (Cont) (See Figure 3-1)

Index No.	Name	Type	Function
6 Cont			1 — Provides proper time constant for high-speed received data 2 — Provides proper time constant for high or medium-speed received data 3 — Provides proper time constant for medium or low-speed received data 4 — Provides proper time constant for low-speed received data (TTY speeds)
7	RX TIMING (S2)	Toggle switch	Selects timing source for the receiver and error counter as follows: In DATA position, causes receiver reference pattern generator and error counter to be timed by internal clock source (VFO or crystal) locked to received data transitions In CLOCK position, selects incoming SCR clock signal as source of timing for receiver reference pattern generator and error counter, and disables VFO phase-lock circuit
8	DATA (J5)	BNC connector	Provides front-panel monitor connection for incoming data from system under test

Table 3-3

ERROR COUNTER (A4) CONTROL, INDICATOR, AND CONNECTOR DESCRIPTIONS (See Figure 3-1)

Index No.	Name	Type	Function
1	BIT ERRORS (A7DS101 thru A7DS106)	Numerical neon display	Displays 6 decades of totalized bit errors
	BLOCK ERRORS (A6DS101 thru (A6DS106)	Numerical neon displays	Displays 6 decades of totalized Blocks in error
	BLOCKS (A5DS101 thru A5DS106)	Numerical neon display	Displays 6 decades of totalized number of blocks received
2	BLOCK LENGTH (S701 thru S704)	Digital thumb-wheel switches	Select block length in 4-digits from one to 9999 bits
	ERR. /BLK	Digital thumb-wheel switch	Selects permissible errors per block from zero to nine
3	ON-OFF-RE-SET ALARM (S708)	3-position toggle switch	Controls latching alarm circuit in each position, as follows: ON – Enables audible channel outage alarm OFF – Disables audible channel outage alarm RESET ALARM (momentary) – Resets channel outage alarm circuit

Table 3-3

ERROR COUNTER (A4) CONTROL, INDICATOR, AND CONNECTOR DESCRIPTIONS (Cont) (See Figure 3-1)

Index No.	Name	Type	Function
4	CHAN. OUTAGE (DS703)	Indicator	Indicates that error rate over ten second period has exceeded 25 percent, activating channel outage alarm circuit
5	RESYNC RESET (S707)	Toggle switch	Resets latching resync alarm circuit
6	RESYNC (DS702)	Indicator	Indicates that pattern synchronization was lost and that resync command was issued
7	COUNT OVERFLOW (DS701)	Indicator	Indicates that any one of or all of displays have exceeded 999, 999
8	RUN-STOP-RESET (S706)	3-position toggle switch	Controls displays in each position, as follows: RUN – Enables displays and display counters STOP – Holds count RESET (momentary) – Resets displays and display counters to zero and resets COUNT OVERFLOW indicator

Table 3-4

POWER SUPPLY (A5) CONTROL AND INDICATOR DESCRIPTIONS (See Figure 3-1)

Index No.	Name	Type	Function
1	POWER (S1)	Toggle switch	Applies primary ac power to Model 600F
2	POWER (DS1)	Indicator	Lights when ac power is applied to Model 600F

Table 3-5

DATA SET ADAPTER (A6) CONTROL, INDICATOR, AND CONNECTOR DESCRIPTIONS (See Figure 3-1)

Index No.	Name	Type	Function
1	INTERFACE (S3)	2-position rotary switch	Selects level converter suitable for interfacing data sets, as follows: E position – Selects level converters for voltage driven data sets I position – Selects level converters for current driven data sets
2	DSR (DS1)	Indicator	Lights to indicate data-set-ready (DSR) condition
3	CS (DS2)	Indicator	Lights to indicate clear-to-send (CS) condition in data set

Table 3-5

DATA SET ADAPTER (A6) CONTROL, INDICATOR, AND CONNECTOR DESCRIPTIONS (Cont) (See Figure 3-1)

Index No.	Name	Type	Function
4	COO (DS3)	Indicator	Indicates carrier-on-off (COO) condition. When lighted indicates carrier-on condition in data set. When not lighted indicates carrier-off condition
5	SQ (DS4)	Indicator	When not lighted, data set indicates that the quality of data being received by Model 600F has degraded seriously. Also does not light when data set is not equipped with an SQ signal
6	MODE (S4)	3-position rotary switch	Selects send-data signal to be sent to data set in each position, as follows: PR – Selects pseudorandom data from pattern generator 0 – Selects steady 0 (+10 v or 25 ma) level 1 – Selects steady 1 (-10 v or 0 ma) level
7	RS (S2)	Toggle switch	When in ON position, provides request-to-send (RS) signal to data set
8	SCTE (TP1)	BNC connector	Monitors serial clock transmit external (SCTE) signal to data set (in parallel with rear connector J7)

Table 3-5

DATA SET ADAPTER (A6) CONTROL, INDICATOR, AND CONNECTOR DESCRIPTIONS (Cont) (See Figure 3-1)

Index No.	Name	Type	Function
9	SCR (TP3)	BNC connector	Monitors serial clock receive (SCR) signal from data set (in parallel with rear connector J7)
10	SCT (TP2)	BNC connector	Monitors serial clock transmit (SCT) signal from data set (in parallel with rear connector J7)
11	RD (TP4)	BNC connector	Monitors receive data (RD) signal from data set (in parallel with rear connector J7)
12	SD (TP5)	BNC connector	Monitors send data (SD) signal to data set (in parallel with rear connector J7)

e. Depress RESYNC RESET switch and let switch return to normal position.

f. Set BLOCK LENGTH Thumbwheels to selected block length (0001 through 9999) and ERR. /BLK thumbwheel to permissible errors per block (p through 9).

3.3.2 OPERATION

In full-duplex operation the pattern generator transmits a pattern through a data set or other device to be tested, and the receiver accepts a pattern generated by a second Model 600F at the other end of the communications link. The transmit and receive functions are independent of each other. The data sets to be tested may be of the synchronous or asynchronous type. A "synchronous" data set is defined here as a data set or modem where the send and receive data bits are accompanied by a synchronous clock signal. The transmit data sub-set may either provide or accept the synchronizing clock signal, whereas the receive data sub-set always provides the clock which is derived from the sending

transmitter. An "asynchronous" data set is a data set or modem in which the send and receive data are not accompanied by a synchronous clock, and where the data rates (bit period) can vary over some specified range. Procedures for operating the Model 600F with combinations of both types are given in the following paragraphs.

3.3.2.1 Internally Timed Synchronous Data Sets. When both the transmit and receive functions of data sets under test are operating synchronously, operate the Model 600F as follows:

a. Set pattern generator TX CLK switch to SCT position. Ensure that send clock signal from the data set is connected to SCT input of Model 600F.

b. Set receiver RX TIMING switch to CLOCK position. Ensure that receive clock signal from data set is connected to SCR input of Model 600F.

c. Set INTERFACE switch to correct position for interface with data set, MODE switch to PR position, and RS switch to ON position.

d. Connect SD output of Model 600F to SD input of data set, and RD input to RD output of data set.

e. Set AUTO-MAN-RESYN switch to AUTO position. If RESYN indicator is lighted, depress RESET switch.

f. Set ON-OFF-RESET ALARM switch to ON.

g. Set RUN-STOP RESET switch to RUN position and note that BLOCKS display indicates number of received data test blocks and that BIT ERRORS and BLOCK ERRORS displays indicate number of bit errors and block errors, respectively, in received data.

3.3.2.2 Externally Timed Synchronous Data Sets. When both the transmit and receive functions of data sets under test are operating synchronously and the transmit function is externally timed, operate the Model 600F as follows:

a. Set pattern generator TX CLK switch to SCTE position.

b. Set RANGE MS switch to one of crystal positions (CR1 or CR2) as required for correct bit rate.

c. Proceed as in steps b through g of paragraph 3.3.2.1.

3.3.2.3 Asynchronous Data Sets. When testing with an asynchronous data set, the Model 600F can normally be used only as a simplex test device to either transmit or to receive at any time since only one internal clock source is available. However, the portion of the test set not utilizing the internal clock may still be used at the same time to operate with a transmit or receive portion of a data set supplying its own clock. These capabilities can be utilized by following procedures a and b. Full duplex tests with asynchronous data sets may be possible in some instances as detailed in procedure c. Procedures for operating the Model 600F with asynchronous data sets are as follows:

a. Transmit to an Asynchronous Data Sub-set and Receive from a Synchronous Data Sub-set.

(1) Set TX CLK switch to SCTE position.

(2) Set RANGE MS switch to one of crystal positions (CR1 or CR2) for desired bit rate of send data. If correct crystal frequency is not available, set RANGE MS switch and vernier dial to correct VFO frequency for bit rate of send data (See Figure 3-2).

(3) Proceed as in steps b through g of paragraph 3.3.2.1.

b. Receive from Asynchronous Data Sub-set and Transmit to an Internally Timed Synchronous Data Sub-set.

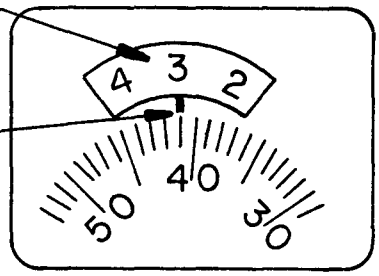
(1) Set RX TIMING switch to DATA position.

(2) Set VFO TIME CONSTANT switch to correct position for bit rate of received data (refer to Table 3-2 for correct position of switch).

(3) Set RANGE MS switch and vernier dial to frequency of received data (see Figure 3-2). Make fine adjustment with vernier dial to bring VFO

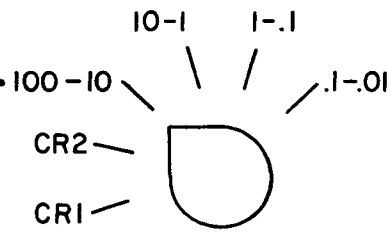
1. Read coarse setting (3) and place a decimal point immediately after it (3.)

2. Read fine setting (41) and insert it after decimal point of coarse setting (3.41).



Vernier Dial

3. Multiply 3.41 by selected range multiplier (10). The reading is thus 34.1 ms. Select multiplier as follows:



RANGE MS switch

RANGE MS	BIT LENGTH (Milliseconds)	BIT RATE (Bits-per-second)	Multiplier
100 - 10	100 to 10	10 to 100	10
10 - 1	10 to 1	100 to 1,000	1
1 - .1	1 to .1	1,000 to 10,000	.1
.1 - .01	.1 to .01	10,000 to 100,000	.01

Figure 3-2. Interpreting Vernier Dial Setting

ERROR meter pointer to center position.

(4) Set TX CLK switch to SCT position.

(5) Proceed as in steps c through g of paragraph 3.3.2.1.

c. Full-duplex Test with Asynchronous Data Sets. In some instances, the Model 600F send data and receiver reference pattern may both be timed by the internally generated clock. The bit rate of send data will be as set for the received data by the RANGE MS switch and vernier dial. The send pattern will jitter because the internal clock is constantly being updated by the received data. However, this mode of operation may be acceptable when both the transmit and receive function of the data sets under test are asynchronous. Procedure for this mode of operation is as follows:

(1) Set TX CLK switch to SCTE position.

(2) Set RX TIMING switch to DATA position.

(3) Set VFO TIME CONSTANT switch to correct position for bit rate of received data.

(4) Set RANGE MS switch and vernier dial to frequency corresponding to bit rate of received data. Make fine adjustment with vernier dial to center VFO ERROR meter pointer.

(5) Proceed as in steps c through g of paragraph 3.3.2.1.

d. Asynchronous Operation Under Noisy Conditions. When the receive function of the data set under test is asynchronous and the received data is abnormally noisy, it may be difficult to establish phase-lock by observing the VFO ERROR meter. At such times, jitter of the meter pointer can mask indications that the VFO is within locking range. The following procedure may help obtain phase lock.

(1) Disable VFO phase-lock action by setting RX TIMING switch to CLOCK position.

(2) Connect received data monitor to vertical input of oscilloscope.

(3) Connect SCTE monitor to sync input of oscilloscope.

NOTE

Ensure that VFO clock rate is approximately the same as received data rate. The pattern displayed on the oscilloscope will drift slowly.

(4) Adjust pattern generator vernier dial until display no longer drifts; both patterns are now in phase.

(5) Enable VFO phase-lock by setting RX TIMING switch to DATA position.

3.3.2.4 Summary of Control Settings. Table 3-6 is a summary of the operating control settings of the Model 600F pattern generator and receiver for the operating procedures given in paragraphs 3.3.2.1 through 3.3.2.3.

Table 3-6

SUMMARY OF CONTROL SETTINGS

Types of Data Sub-sets Under Test	Settings Required for Transmitting		Settings Required for Receiving	
	Pattern Generator		Receiver	
	TX CLK Set To	RANGE MS Set To	RX TIMING Set To	VFO TIME CONSTANT Set To
TX: Synchronous, Internally Timed RX: Synchronous	SCT	----	CLOCK	----
TX: Synchronous, Externally Timed RX: Synchronous	SCTE	CR1 or CR 2	CLOCK	----
TX: Asynchronous RX: Synchronous	SCTE	Desired TX Test Data Rate (Period)	CLOCK	----
TX: Synchronous, Internally Timed RX: Asynchronous	SCT	Desired RX Test Data Rate #	DATA	Positions 1, 2, 3 or 4 Depending on Data Rate
TX: Asynchronous* RX: Asynchronous	SCTE	Desired TX and RX Test Data Rate**	DATA	Positions 1, 2, 3 or 4 Depending on Data Rate

#Setting required for receiving
*Restricted Use - See Text
**Setting required for transmitting and receiving

SECTION 4

PRINCIPLES OF OPERATION

4.1 INTRODUCTION

In this section, operation of each of the five modules comprising the Model 600F is described at both a functional and a circuit level. The functional description of each module other than the power supply module is keyed to the system block diagram in Figure 6-1. The detailed, circuit level, description of the circuits is keyed to the schematic diagrams in Section 6 of this manual.

4.2 FUNCTIONAL DESCRIPTION

The following paragraphs provide a functional description of each module in the Model 600F.

4.2.1 PATTERN GENERATOR

The pattern generator essentially contains a variable frequency oscillator, a series of frequency dividers, two crystal oscillators with an associated phase-lock circuit, a pseudorandom bit generator, and an error test generator. The pattern generator provides a pseudorandom pattern sequence which is 2047 bits in length. The unit has an operating range from 10 to 150,000 bits per second (bps), and can be timed from either an internal or an external drive source as selected by a front panel TX CLK switch. When the SCTE position is selected, a choice of one of two crystal-controlled oscillators or a variable frequency oscillator is available for driving a system of binary counters. The counters supply internal clock (shift) pulses for driving the shift register section of the pseudorandom pattern generator. A front panel RANGE MS switch selects the type of oscillator and appropriate counter sequence to produce the desired output pattern rate.

4.2.1.1 Variable Frequency Oscillator. The variable frequency oscillator (VFO) can provide the internal main and quad clock signals at rates from 10 to 100,000 bps in four ranges selectable by means of the front panel RANGE MS switch. Each range of the switch is continuously adjustable by means of a front panel vernier dial. Dial readings are in milliseconds.

The main clock signal is used to control the output pattern rate when the TX CLK switch is set to the SCTE position. The main and quad clock are used as receive clock signals in the receiver module when the RX TIMING switch is set to DATA position. When the VFO supplies the receive clock signal, automatic frequency control of the VFO is provided by the receiver section which derives a clock signal from the data to continuously correct the VFO so that its output is always in the proper phase relationship with the incoming data. Output signals from the VFO are routed to the frequency divider of the pattern generator.

4.2.1.2 Crystal Oscillator and Phase-Lock Circuit. Two crystal oscillator circuits provide two pre-determined internal main and quad clock rates within the range from 300 to 7200 bps. These clock rates are selectable by means of the front panel RANGE MS switch. Switch position CR1 enables crystal oscillator 1, and position CR2 enables crystal oscillator 2. The fundamental frequency of the quartz crystal in crystal oscillator 1 and crystal oscillator 2 is 80 times the output clock rate. The output of the selected crystal oscillator is applied to an OR gate whose output is applied to a phase-lock circuit. The output of the phase-lock circuit is applied to a frequency divider circuit which provides the desired clock rate.

The crystal oscillators may be used to control the send data rate or the receiver reference pattern rate. When used to control the receiver reference pattern rate, the RX TIMING switch is set to DATA position. The crystal oscillator phase-lock circuit is enabled only when the RX TIMING is set to the DATA position.

The phase-lock circuit basically contains add and delete circuits which function to add or delete pulses at the crystal frequency divider. The overall effect of this action is to bring the internal time base into correct phase alignment with the receive data. In operation, the internal (quad) clock is routed to the phase-lock circuits for comparison with the receive data. Any phase difference between these signals is recognized and stored by either an early or a late flip-flop. If the receive data leads the quad clock, an early flip-flop is set. The next zero-going transition of the quad clock then resets the early flip-flop. As a result, the early flip-flop sets an add flip-flop which supplies an additional pulse to the frequency divider.

If the receive data lags the quad clock, a late flip-flop is set. The next zero-going transition of the quad clock then resets the late flip-flop. As a result, the late flip-flop sets a delete flip-flop which prevents the

drive gate from passing the next oscillator pulse to the frequency divider.

4.2.1.3 Frequency Divider. The frequency divider consists of decade counters and three associated divide-by-two counters. The divider reduces the output frequency of the VFO or a selected crystal oscillator by the appropriate factor to produce main and quad clock signals at the rate selected by the RANGE MS switch. When this switch is placed in the 100-10 position, counters #1 through #6 are used to divide the VFO output by a factor of 4000. When the RANGE MS switch is in the 10-1 position, counters #1, #2, #4, #5, and #6 divide the VFO output by a factor of 400. The 1-.1 position of the RANGE MS switch selects counters #1, #4, #5, and #6 to divide the VFO output by a factor of 40. Finally, the .1-.01 position selects counters #4 through #6 to reduce the VFO output by a factor of 4.

When the RANGE MS switch is placed in the CR1 or CR2 position, counters #1, #4, #5, and #6 divide the output of the phase-lock circuit by a factor of 40. Since the crystal phase-lock circuit also contains a divide-by-two counter, the total division factor is 80.

The output of the frequency divider is obtained from counter flip-flops #5 and #6. These counters are triggered by opposite phase outputs from divide-by-two counter #4. As a result, counter flip-flops #5 and #6 provide outputs which are 90 degrees out of phase with respect to each other.

Counter #5 provides a main clock signal which is routed to the front panel SCTE connector, the receiver module, the data set adapter module, and the front panel TX CLK switch.

Counter #6 provides a quad clock signal which is connected to the crystal oscillator phase-lock circuit, and to the VFO phase-lock flip-flop in the receiver module. By means of a phase-locking process, counter #5 is maintained at a 90 degree phase lagging condition with respect to incoming data; whereas, counter #6 is maintained at an in-phase condition with respect to incoming data.

4.2.1.4 Pseudorandom Bit Generator. The pseudorandom bit generator consists of an eleven-stage shift register, a feedback control gate, and an Exclusive-OR circuit. Together, the three circuit elements form an m-sequence, pseudorandom bit generator which provides a pattern length of 2047 bits. The feedback loop between the register output and

input is by way of the register feedback control gate. The output from the pseudorandom bit generator is amplified and connected to the SD BNC connector of the pattern generator, and to a driver in the data set adapter.

4.2.1.5 Error Test Generator. The error test circuit consists of an error test gate, an error AND gate, an error flip-flop, and a front-panel error test switch. The error test circuit provides either a single, unrepeated frame error bit or one error bit every 2047-bit frame, as selected by the INSERT ERRORS-OFF-SINGLE switch. Essentially, this circuit assumes control of the output NOR gate during the time of the frame error bit. When the INSERT ERRORS-OFF-SINGLE switch is in the OFF position, the error flip-flop is reset, disabling the error AND gate and allowing the Exclusive-OR gate to control the output NOR gate. When the switch is in the SINGLE (momentary-contact) position, the error flip-flop is set, enabling the output AND gate and allowing the frame pulse to appear at the output NOR gate. The frame pulse causes the output of the NOR gate to assume the wrong polarity for the time of one bit. The trailing edge of the frame pulse resets the error flip-flop, disabling the AND gate. Operation of the error test circuit when the switch is in the INSERT ERRORS position is the same as in the SINGLE position except that the error flip-flop remains set, thus allowing each frame pulse to produce an output error.

4.2.2 RECEIVER MODULE

The receiver module contains a VFO phase-lock circuit, data and clock input slicers, a receive pattern generator, error detection circuits, pattern resynchronizing circuits, and a delayed clock generator. The receiver functions to establish pattern synchronization between the reference pseudorandom bit pattern and the received data, to compare the received data bit-by-bit with the reference pattern for errors, and to generate error pulses for readout by the error counter module. When serial clock receive (SCR) is not available, as in the case when operating with asynchronous data sets, the receiver also functions in conjunction with the oscillator in the pattern generator to produce an internal clock signal, bit-synchronized to the incoming data.

4.2.2.1 AFC Phase-Lock Circuit. The automatic frequency control (AFC) phase-lock circuit, consisting of a flip-flop, an Exclusive-OR circuit, a time constant switch, and an integrator circuit, functions only when the RX TIMING switch is set to DATA position. The phase-lock circuit compares the phase of the incoming data with the phase of

the internal clock. Differences in phase are integrated, and the resultant dc level is applied to the VFO in the pattern generator as a correction signal. The phase-lock operation (a form of automatic frequency control) is a continuous process that maintains the internal timebase in proper phase alignment with the incoming data. A front panel meter on the receiver module provides a visual indication of phase lock.

When the RX TIMING switch is set to the DATA position, the AFC enable gate is turned on, and received data signals shaped by the data slicer are routed to the phase-lock flip-flop input. The phase-lock flip-flop is set by the received data, and reset by the internal quad clock, thereby producing two phases for the phase-lock Exclusive-OR circuit. Simultaneously, two phases from the internal main clock are also applied to the Exclusive-OR circuit. When the received data is in phase with the quad clock, the Exclusive-OR output is a squarewave with a 50 percent duty cycle. Any phase shift between the received data and quad clock produces a change in duty cycle at the output of the Exclusive-OR circuit. The resultant signal is applied to the VFO control integrator by way of the contacts of the VFO TIME CONSTANT switch.

The VFO control integrator functions with the VFO TIME CONSTANT switch to control the rate of frequency tracking of the VFO. Positions 1 (fast) through 4 (slow) of the switch select integrator time constants in accordance with the rate and quality of received data.

4.2.2.2 Receive Reference Pattern Generator. The receive reference pattern generator consists of a shift register, an Exclusive-OR gate and a lock-up counter. The pattern generator produces a reference pattern 2047 bits in length, identical to the pattern generated in the pattern generator module. This pattern, as in all other circuits in the receiver module, can be timed from either the internal main clock or an external data set, as selected by the front panel RX TIMING switch. The generated pattern is inserted into the error detection circuits for comparison with the received test pattern. The lock-up counter prevents an all zero lock-up from occurring in the shift register.

4.2.2.3 Delayed Clock Generator. The delayed clock generator produces a clock signal delayed by 2 microseconds from the clock selected by the front panel RX TIMING switch. The delayed clock signal is used in the receiver module to sample the error comparator output, and to clock out error pulses through the error flip-flop. It is also used in the error counter module to process the error pulses in the counter display control circuit, and to generate resync commands in the re-

cognizer circuits.

4.2.2.4 Error Detection Circuits. The error detection circuits consist of an error comparator circuit, an error flip-flop, and a sample pulse generator. The error detection circuits supply pulses to the error counter module whenever data bits in the received test pattern do not agree with the internally generated reference pattern. Error pulses can be generated at the same rate as the receive clock (up to 150 kbs).

The error comparator is an Exclusive-OR gate which provides a positive going pulse when a bit in the received test pattern disagrees with the corresponding bit in the internal reference pattern. Output pulses of the Exclusive-OR gate are sampled near the center of each pulse by pulses from the sample pulse generator to set the error flip-flop when an error exists. The output of the error flip-flop is routed to the error counter module by way of the error inhibit gate and level converters.

4.2.2.5 Pattern Synchronizing Circuit. The pattern synchronizing circuit consists of a feedback control logic circuit, a sync counter, and a data resynchronizing flip-flop. The synchronizing circuit synchronizes the reference pattern generated in the receiver with the incoming data pattern, by feeding the data pattern into the shift register of the pattern generator. The error detection circuit is used as discussed in paragraph 4.2.2.4 to detect errors between the pattern generator output and the incoming data pattern. The sync counter counts bit agreements and sets the feedback control logic through the data resynchronizing flip-flop when 16 consecutive bit agreements have occurred.

The resynchronizing flip-flop can be set either automatically or manually by means of a front panel AUTO-MAN-RESYNC switch. In the AUTO position, the switch permits control from the error counter module resync decision logic to set the flip-flop. The MAN (manual) switch position disables the inputs to the resynchronization flip-flop so that no resynchronization can take place. When the RESYNC (momentary) switch position is selected, the resynchronization flip-flop is set to initiate pattern synchronization.

A front-panel SYNC ALARM indicator lights when the resynchronization flip-flop is set to indicate that pattern resynchronization is in progress.

4.2.3 ERROR COUNTER MODULE

The primary function of the Model 1225 Error Counter Module is to provide reliable resynchronization commands to the Model 600F during specified modes of operation and error rate conditions. It provides a visual display of bit errors, block errors, and total blocks received. In addition, it provides decade switches to establish block length and permissible errors per block, and incorporates test monitoring circuitry which, by means of indicators and audible alarm, indicates conditions of panel display overflow, transmission channel outage, or resync command issuance.

Printed circuit boards contained in the error counter module are: three counter display boards, a counter display control board, a recognizer board, a translator board, and a power supply board which supplies all dc voltages to the module. These printed circuit boards are segregated so that all related functions are contained on the same board. A functional description of each board, keyed to the functional diagram in Figure 4-1, is contained in the following paragraphs.

4.2.3.1 Counter Display Boards. The counter display boards comprise the bit error, block error, and block counters and displays. Each board is composed of six decade counters capable of counting from 000,000 through 999,999. The decade counters feed six BCD-to-decimal decoders which in turn drive six neon readout tubes.

Each of the counter display boards contain a common reset input to the decade counters, and an overflow circuit which detects the trailing edge of the most significant bit to indicate by means of a front panel COUNT OVERFLOW indicator that the counter has exceeded 999,999. The decade counters and COUNT OVERFLOW indicator are reset by setting the front panel RUN-STOP-RESET switch to the RESET (momentary) position.

4.2.3.2 Counter Display Control Board. The counter display control board contains the following circuits: display mode control, block length detector, error block enable, and counter control.

The display mode control circuit allows two modes of operation of the counters during resync period. The two modes are selected by means of the AUTO-CONT switch mounted on the board. When the switch is set to AUTO position, all inputs to the block length detector, error block enable, and bit-error counter are automatically inhibited during

resync period. When the switch is set to CONT position, an artificial 50 percent error rate is introduced to the block error enable and bit-error counter. Dependent upon this switch position, either all display counters are held at their present counts during a resync period or all counters run normally except the 50 percent artificial error rate takes precedence over the normal incoming error rate. This is accomplished by sensing the resync flip-flop for a "true" condition.

The block length detector is composed of four decade counters in conjunction with four BCD thumbwheel switches which are interconnected so as to detect a dialed, four-digit number. The counter then counts to the dialed number. As the number is reached and detected, the counter is reset and an output (through associated gating) yields a pulse of one-half clock time to the block counter. The range of the block length of zero (0000) is essentially an undefined state and will yield the same results as a block length of 0001.

The error block enable circuit is a decade counter which counts and recognizes the number of bit-errors selected on a BCD thumbwheel switch. In operation, once the dialed number has been reached, the system is armed to detect the next bit-error (that is, exceeding the number dialed by one) and to give an output to the block error counter through associated circuitry similar to the block length detector. The thumbwheel switch thus designates the number of errors permitted in any given block.

The counter control circuit is a gating network controlled by the front-panel RUN-STOP-RESET switch. This gating network enables or disables the inputs to the block, block-error, and bit-error counters; the RUN position enables the three inputs; the STOP position disables the three inputs; and the RESET position clears the accumulated counts.

4.2.3.3 Outage Indicator Board. The outage indicator board contains the channel outage detector circuit, channel outage indicator circuit, and latching alarm/driver circuits for the RESYNC and OVERFLOW indicators.

In the channel outage detector circuit, an errors integrator circuit receives "true" error pulses and integrates the power of each pulse (indirectly proportional to speed). The integrator is allowed to run for 10 seconds and is then reset by a ten-second unijunction relaxation oscillator which serves to reset the integrator and provide a clock pulse for the non-latching indicator. The latching version of the channel outage indicator circuit consists of an R-S flip-flop which serves both as a latch and driver for the CHANNEL OUTAGE indicator and the audible

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alarm circuit. The latching function is reset by means of a front panel ON-OFF-RESET switch.

The channel outage alarm is triggered by a NPN buffer amplifier and a PNP clamp circuit to detect a 5-volt trigger level reached by the integrator. The cycle is completed as the unlatched alarm is clocked. The output is then fed to an indicator circuit on the board.

4.2.3.4 Recognizer Board. The recognizer board contains the decision logic circuitry which issues a pattern resync command to the receiver during specified modes of operation and error rate conditions. It monitors four categories of incoming line patterns as follows:

a. An incoming pseudorandom pattern containing bit errors which have an error probability of from 0.00 to 0.25.

b. An incoming pseudorandom pattern containing bit errors which have an error probability of from 0.00 to 0.25 with one error burst interspersed in every 2000 bit segment. These error bursts have bit error probabilities in the range of 0.25 to 0.50.

c. An incoming pseudorandom pattern containing bit errors with a probability of from 0.25 to 0.50. This may include a continuous (longer than 2000 bits) condition of 0.50 bit error probability, in which case the received data can be considered truly random.

d. An incoming pattern which is continuously fixed at either all "0's," all "1's," or repeated "1000" patterns for periods longer than 2000 bits. These fixed patterns are not corrupted by noise.

Under signal condition a, the probability of the recognizer board issuing a resync command when a true loss of synchronization has occurred in the receiver module is 0.99 or higher.

Under signal conditions a and d, the probability of the recognizer board issuing a false resync command when, in fact, the receiver has not lost synchronization is 0.01 or less for any twenty-four hour continuous test at 100,000 bits per second.

Under signal condition b, the probability of the recognizer board issuing

a false resync command is 0.01 or less per error burst.

Under signal condition c, the probability of the recognizer board issuing a false resync command is 0.01 or less for continuous periods of 1,000,000 bits.

When an out-of-sync condition does exist, the decision time for the recognizer board to react when bit-error probabilities are constant at 0.00 is the time required for 100 bits to be sampled. When bit-errors are occurring with a probability greater than 0.00, and equal to or less than 0.25, the decision time to issue the resync command (in a true out-of-sync condition) is the time required for not more than 2000 bits to be sampled.

This latter condition is determined by examining the output of the predictor, which generates a predictor error whenever the current received bit agrees with the Exclusive-OR of the ninth and eleventh preceding bits. The predictor errors and receiver error pulses are used by two systems which operate in parallel. One responds in 100 bits (see Figure 6-11) or less when the pseudorandom pattern is not corrupted by noise; the other responds in 2000 bits or less with a probability of 0.99 as long as the individual bit-error probability is 0.25 or less.

When uncorrupted pseudorandom data persists for 100 bits, 89 "valid" (predictor-error-free) bits will occur. The bit counter will overflow and a resync command will be issued if both error pulses and logical "0's" occurred during the same 89 bits. If the overflow was caused by 100 consecutive logical "1's", the output of the repeating "1" detector inhibits resync commands and holds the 2000 bit system reset until a logical "0" occurs in the data.

The 2000 bit system makes its decision on the basis of error-pulse and predictor error counts during the 1750 bit tests. To insure response within 2000 bits after a slip-sync, tests are aborted after 250 bits if the error-pulse rate is low enough to guarantee an in-sync condition with a probability of 0.998. When trouble is detected during a 250 bit test, the tests, which are already in progress, are allowed to run for the full 1750 bits. The predictor-error threshold, above which the data is considered non-pseudorandom, is high enough to insure a conditional probability of resync of 0.992 or more with individual bit-error probabilities of 0.25 or less. This threshold is also low enough to insure that the probability of not reaching it with truly random data is

about .0072. If the pseudorandomness test is passed, a resync command is issued as long as the error pulse rate has remained high enough during the simultaneous 1750-bit error pulse test. This latter requirement prevents false resync commands following error bursts long enough to be caught by the 250-bit trouble-detecting test, but too short to cause a failure of the 1750-bit pseudorandomness test.

If the pseudorandomness test is failed, it is probably due to truly random data persisting for over 1750 bits. The system has already incurred a .0072 probability of false resync. Since it is required to withstand 1,000,000 bits of truly random data with an overall false resync probability of 0.01, the 2000-bit system must alter its resync criteria until it can be reasonably sure that the extended error burst of truly random data has ended. This is done by incrementing a scale-of-three up/down counter whenever a pseudorandomness test is failed and decrementing it when one is passed. When this counter returns to zero, the system stops performing pseudorandomness tests, and returns to the 250-bit trouble-detecting tests. The counter is never permitted to overflow, so that following an extended error burst, the system will recover in 3400 to 5100 bits with a probability of over 0.984 as long as the individual bit-error probability falls to 0.25 or less.

Continuous logical "0's" will appear like an error burst to the system, and the same recovery time performance applies following restoration of valid data. A resync command will be issued 1750 bits after recovery from this condition with a probability of 0.99 or higher. If the individual bit-error probability falls to .05 or less, the 100-bit system will usually respond first. Since the resync flip-flop completely resets the 2000-bit system, it will resume 250-bit trouble-detecting tests after resync is complete. The 2000-bit system is also held reset by the output of the repeating "1" and repeating "1000" detectors, since the system considers such data to be pseudorandom and would otherwise issue false resync commands.

4.2.3.5 Translator Board. The translator board performs all input/output functions of the interface between the error counter module and the receiver module.

The translator board consists of five input translators which feed the balance of the error counter module circuitry. The translators perform voltage level conditioning (+5 volts is a logical "1" and 0 volts is a logical "0") for the following inputs: selected inverted clock, quad clock, reference data, bit errors, and resync flip-flop output.

The translator board, further, consists of six output translators, five of which are designed to operate an external printer, and the last which provides the voltage level shift for the resync command line.

4.2.3.6 Power Supply. The power supply board provides the error counter module with regulated +5 vdc at a nominal current of 2.0 amperes for the logic and input translators. A high voltage regulator provides +200 vdc at a nominal current of 24 ma for the readout tubes.

4.2.4 POWER SUPPLY MODULE

The Model 600 power supply module contains rectifier sections which provide operating dc voltages to the pattern generator, the receiver, and the data set adapter modules. In addition, it provides the Model 1225 Error Counter Module with unfiltered -12 vdc for the channel outage audible alarm circuit, filtered +12 vdc for the outage indicator error integrator circuit, and filtered -12 vdc for the resync command level converter circuit. Primary ac power is applied to the module, and to the Model 1225 power supply, by means of a front panel POWER ON switch.

4.2.5 DATA SET ADAPTER

The data set adapter essentially consists of level converters which provide input and output interface for voltage or current driven data sets. The data set adapter also contains indicator lamps and drivers, an INTERFACE switch which controls the operating mode of the level converters, a MODE switch, and an RS (request-to-send) switch. Front panel BNC connectors are provided to monitor data and clock signals transmitted and received by the Model 600F.

Operation of the level converts on either voltage (E) or current (I) mode is controlled by the front panel INTERFACE switch. When the switch is set to E position, the send level converters translate 0- and -10-volt logic levels from the Model 600F to +6 and -6 volts, respectively, for interface with voltage driven data sets, and the receive level converters translate +6- and -6-volt levels from voltage driven data sets to 0- and -10-volt levels, respectively. When the switch is set to I position, the send level converters change 0- and -10-volt levels to currents greater than 23 ma and less than 5 ma respectively, for interface with current driven data sets. The process is reversed for signals received by the Model 600F.

Signals processed by the level converters consist of those transmitted to data sets and those received from data sets. Transmitted signals are serial clock transmit external (SCTE) and send data (SD). Received signals are serial clock receive (SCR), receive data (RD), and serial clock transmit (SCT). The SCR and RD signals are routed to the receiver module, and the SCT signal is routed to the pattern generator module.

Lamp drivers are provided to indicate data-set-ready (DSR), clear-to-send (CS), carrier on-off (COO), and signal-quality (SQ) conditions in the data set under test.

The MODE switch controls selection of transmitted data signals. When the switch is set to PR position, pseudorandom data at 10 to 150,000 bits per second from the pattern generator is selected for transmission to the data set. The 0 position selects transmission of all "0's", and the 1 position selects transmission of all "1's."

The RS switch provides a request signal to the data set under test. When the switch is set to ON position, +6 volts is placed on the request-to-send line to the data set. This causes the data set to return a clear-to-send (CS) signal to the Model 600F. As a result, the CS lamp glows, indicating that data transmission may begin. When the RS switch is set to OFF position, -6 volts is placed on the line. The CS lamp is then turned off by the data set to indicate that data will not be accepted.

4.3 DETAILED CIRCUIT DESCRIPTION

4.3.1 PATTERN GENERATOR

The pattern generator module consists of the following items: two crystal oscillators, a phase-lock circuit for the crystal oscillators, a variable frequency oscillator (VFO), a frequency divider, a pseudorandom pattern generator, a frame pulse circuit, and an error test generator. A detailed circuit description of each item is presented in the following paragraphs.

4.3.1.1 Crystal Oscillators. See Figure 6-1. Transistor stages Q1-Q2 and Q3-Q4 comprise two functionally identical series-resonant crystal oscillators designed to operate over a range of 24 kHz to 576 kHz. Either oscillator is selectable by means of the front panel RANGE MS switch. The CR1 position of this switch selects the Q1-Q2 circuit, and the CR2 position selects the Q3-Q4 circuit. Crystals Y1 and Y2 are of

the plug-in type, and their respective frequencies are determined by the data rate of the system being tested. The proper crystal frequency is obtained by multiplying the data rate by a factor of 80. Capacitors CV1 and CV2 are used to trim to the exact frequency.

Positive-going clock pulses from the selected oscillator circuit are connected to transistor OR gate Q5. The resultant phase 2 clock at the collector of Q5 resets delete flip-flop Q17-Q18. Stage Q17 of this flip-flop then provides a "zero" level signal to one input of drive gate Q19. (The delete flip-flop is described in a later paragraph.) Simultaneously, the phase 2 clock at the collector of Q5 is routed through inverter Q6 to become the phase 1 clock output. The phase 1 clock is then applied to the other input of drive gate Q19. This operation turns on Q19 and supplies drive pulses to a frequency divider circuit.

Transistor stages Q22-Q23 comprise a flip-flop divider circuit which halves the frequency of the selected crystal oscillator output. The resultant output at the collector of Q23 is routed through pin L to a two-input NOR gate located in the VFO section of the pattern generator. The other input to this NOR gate consists of the VFO output. (Both circuits are described in a later paragraph.) The output of the divider stage at the collector of Q23 is clamped to the "zero" level whenever VFO operation is selected. The clamping voltage is applied through pin K to the base of Q23 when the front-panel RANGE MS switch is not set to one of the crystal positions.

4.3.1.2 Crystal Oscillator Phase-Lock Circuit. See Figure 6-1. The crystal oscillator phase-lock circuit consists of add and delete circuits which add or delete drive pulses to the crystal frequency divider. The add circuits consist of add flip-flop Q20-Q21, add gate R40-C8-CR4, early flip-flop Q8-Q9, and early control gate Q10. The delete circuits consist of delete flip-flop Q17-Q18, delete gate R39-C7-CR3, late flip-flop Q13-Q14, and late control gate Q15. A noise immunity gate, Q16, is common to the add and delete circuits. This gate functions to prevent instability (jitter) of the divider signal during high noise periods.

Input signals to the crystal phase-lock circuit are negative-going quadrature clock pulses (abbreviated quad clock) from the divider section of the pattern generator and external positive-going timing crossover pulses from the phase-lock flip-flop in the receiver. The quad clock, which is applied at pin A, turns off inverter stage Q12. The resultant positive-going output from Q12 is simultaneously applied to the base of early control gate Q10, to the base of inverter Q7, and to the junction of C13-C14.

Consider, now, the input at pin M. This input consists of the external timing crossover pulses. If it is assumed that no crossover pulses are being received, the input at pin M is at the "zero" level and inverter Q11 remains off. Transistor Q11 therefore supplies a positive voltage to the junction of R75-R81. The overall conditions at this time are as follows: Q11 and Q12 are off, Q7-Q10-Q15 are on, the early and late flip-flops are reset to left side on, noise immunity gate Q16 is on, and the circuits are primed for the addition or deletion of pulses. First, the latter operation is described with the aid of the waveforms in Figure 4-2.

Pulses are deleted at the output of the crystal frequency divider (pin L) whenever the external timing crossover pulses are late with respect to the quad clock. In other words, transistor Q12 is off when the crossover pulse arrives at pin M. In operation, a positive-going late crossover pulse turns on Q11, turns off late control gate Q15, and thus sets late flip-flop Q13-Q14 to left side off. No change takes place in the early circuits at this time.

The set condition of the late flip-flop produces a positive voltage at the collector of Q14 which charges delete gate capacitor C7. The corresponding zero level at Q13 does not affect the on state of Q16, since a positive level is still maintained at its base by early flip-flop stage Q8. These conditions remain stable until the late flip-flop is reset.

At this point, it is necessary to discuss again the action of drive gate Q19 as controlled by phases 1 and 2 of the oscillator output. Drive gate Q19 is controlled directly by the phase 1 signal and indirectly (via the delete flip-flop) by the phase 2 signal. Normally, the phase 2 signal resets the delete flip-flop, thereby maintaining a constant "zero" level at the collector of Q17. At the same time, the phase 1 signal at the collector of Q6 alternates from "zero" to positive. As a result, drive gate Q19 is turned on and off in step with the phase 1 transitions, and the divider output is produced as explained previously.

In Figure 4-2, note the relationship between the phase 1 pulses and the output of drive gate Q19. Ideally, these two signals should follow each other in an inverted relationship. In practice, however, pulse deletions occur at Q19 because of the action of the delete and late flip-flops.

Thus far, the delete flip-flop has been reset and the late flip-flop has been set. When the late flip-flop is again reset, a zero-going pulse passes through the delete gate and sets the delete flip-flop to right side

off. The resultant positive level at the collector of Q17 then holds drive gate Q19 on until one zero-going transition of the phase 1 clock has occurred. An expanded view of the delete action is also shown in Figure 4-2. The overall effect of this operation is that a pulse has been deleted at the crystal divider and the phase of the internal clock is retarded by 1/80th of an output bit. The delete process is repeated for each late crossover pulse until the incoming and internal clocks are properly phased.

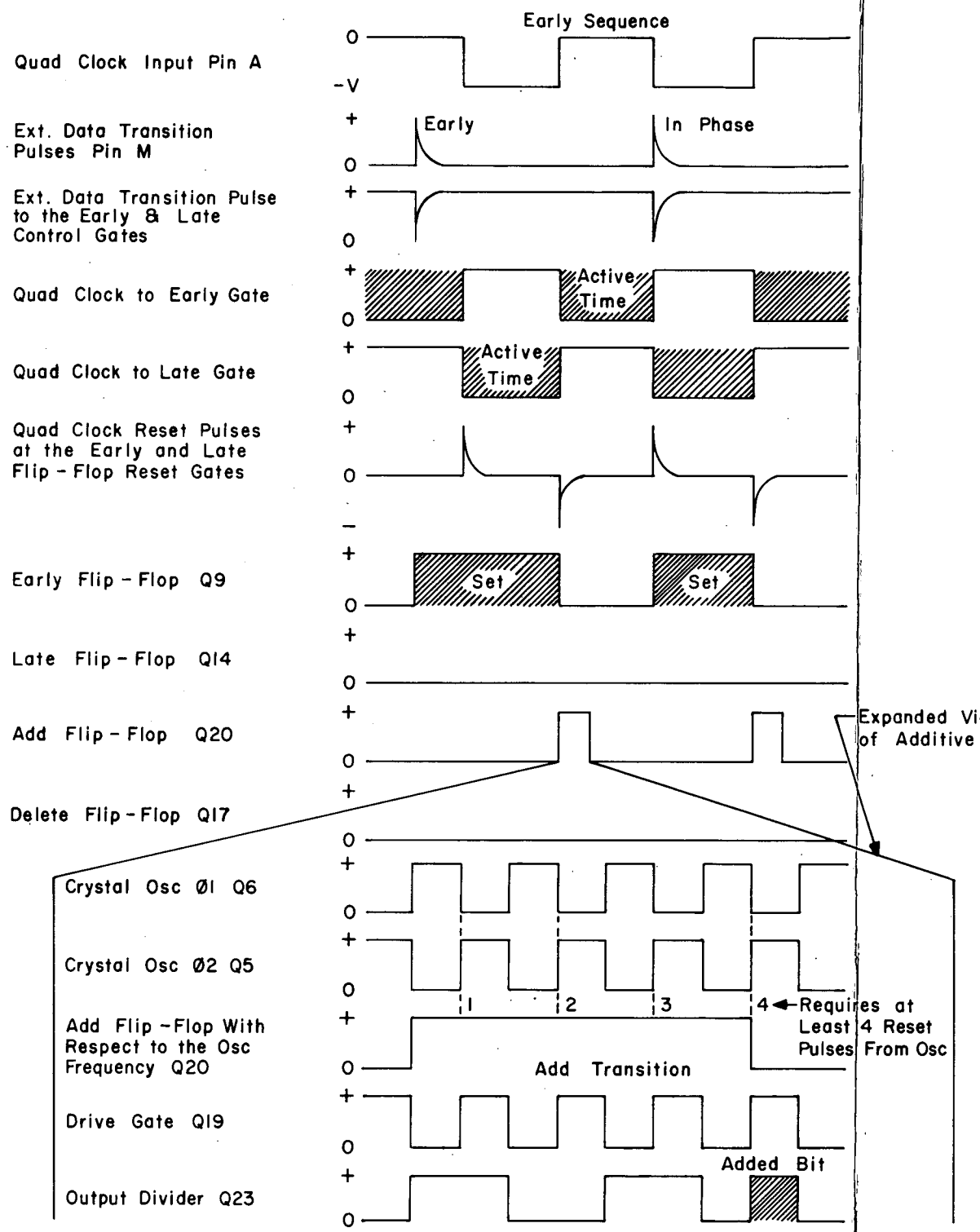
Pulses are added to the crystal frequency divider output whenever the external timing crossover pulses are early with respect to the quad clock. That is, transistor Q12 is on when the crossover pulse arrives at pin M. In operation, a positive-going early crossover pulse turns on Q11, turns off early control gate Q10, and thus sets early flip-flop Q9-Q10 to left side off. No change takes place in the late circuits at this time.

The set condition of the early flip-flop produces a positive voltage at the collector of Q9 which charges add gate capacitor C8. The corresponding zero level at Q8 does not affect the on state of Q16, since a positive level is still maintained at its base by late flip-flop stage Q13. These conditions remain stable until the early flip-flop is reset.

When the early flip-flop is again reset, a zero-going pulse passes through the add gate and sets the add flip-flop to right side off. This operation, along with an expanded view of the ensuing additive action, is shown in Figure 4-2. As long as the add flip-flop is set, phase 1 clock pulses continue to drive the crystal divider by way of Q19. Normally, four or more phase 1 pulses are required to reset the add flip-flop. The reason for this is that a longer time constant is used in the reset gate of Q21 to provide sufficient discharge time for the add gate in the Q20 set side.

After reset gate capacitor C6 accumulates a sufficient charge, the add flip-flop is reset, and a zero-going pulse at the collector of Q20 produces another pulse from the crystal divider. It is obvious that this pulse is an extra pulse, since the phase 1 signal is at the mid-bit transition point with respect to the divider output. (Only the positive-going portion of the phase 1 clock pulses produces a transition at the divider output.) The overall effect of this operation is that a pulse has been added to the divider output, and the phase of the internal clock is advanced by 1/80th of an output bit. The add process is repeated for each early crossover pulse until the incoming and internal clocks are properly phased.

FOLDOUT FRAME 1



FOLDOUT FRAME 2

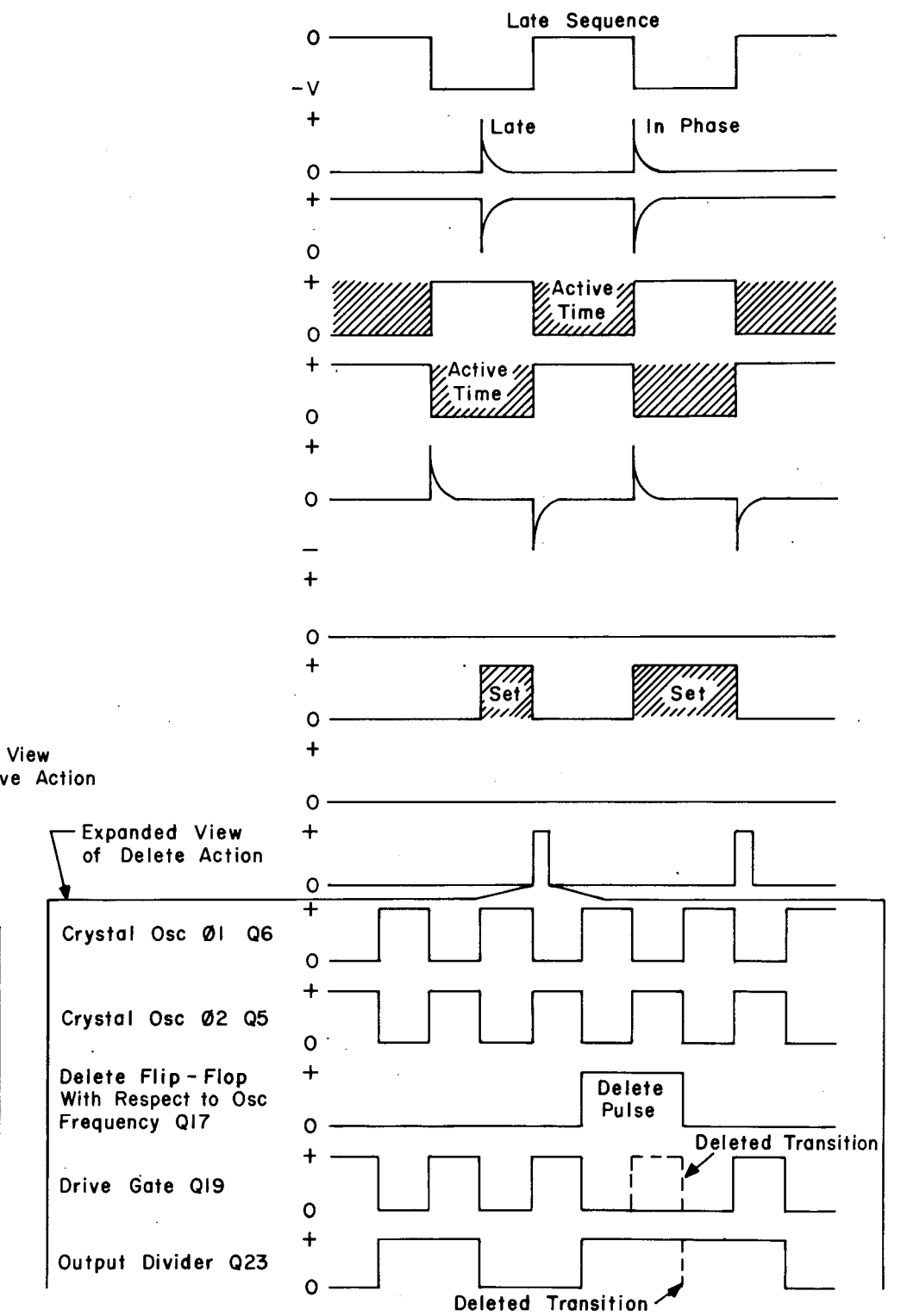


Figure 4-2. Crystal Phase-Lock Waveforms

Noise immunity gate Q16 functions to remove jitter from the crystal divider output during periods when the input signals are excessively noisy. At such times, if the noise level is sufficiently high, both the early and late flip-flops will be set simultaneously, and Q16 will be turned off. The resultant positive level at the collector of Q16 blocks the add and delete gates, thereby preventing unwanted transitions in the divider output.

4.3.1.3 Variable Frequency Oscillator. See Figure 6-2. The variable frequency oscillator (VFO) comprises transistor stages Q3 through Q7. Stages Q3, Q4, and Q5 form a resistance-capacitance oscillator circuit, and stages Q6, Q7 function as coupling elements. The oscillator frequency is continuously variable from 40 kHz to 400 kHz by means of a front panel mounted 10-turn 50 K-ohm potentiometer (R1, Figure 6-6). A vernier dial is used to adjust this potentiometer, thereby providing accurate tuning of the oscillator. Initial calibration of the oscillator is accomplished by means of ratio potentiometer R35 and frequency potentiometer R20.

The VFO is enabled by +12 volts applied to pin K when the front panel RANGE MS switch is set to any position except the two crystal positions. Assume that when the VFO is enabled, Q4 is off and Q5 is on. The control input signal at pin B is supplied to the base of Q4 from the VFO phase-lock circuit located in the receiver module. This control signal, which varies in response to phase differences between the internal and external timing signals, is routed to Q4 via the 10-turn potentiometer, R1 (Figure 6-6), and the ratio potentiometer, R35. As a result, capacitor C1 begins to charge until it reaches the turn-on potential of Q4. When this point is reached, Q5 is turned off and Q3 is turned on, thereby discharging C1. The cycle then repeats itself. Transistor stage Q3 also functions to supply the VFO output to NOR gate Q2.

Transistor stage Q2 is a NOR gate which functions to route either the VFO or the crystal divider output to the frequency divider portion of the pattern generator. In the VFO mode, the crystal divider input at pin C is grounded, and the operating point for Q2 is established by R7-R8 and the collector level of Q3. When Q3 is off, its positive collector level holds off Q2 via diode CR19. When Q3 is on, the negative-going VFO pulses back-bias CR19, thereby permitting Q2 to turn on. In this manner, the VFO output is routed to inhibit gate Q1 and to the frequency divider section of the pattern generator.

In the crystal oscillator mode, pulses at pin C from the crystal divider

F

alternately turn oscillator NOR gate Q2 on and off. In this manner, the crystal oscillator output is also routed to inhibit gate Q1 and to the frequency divider section of the pattern generator.

Inhibit gate Q1 controls the VFO output to a clock NOR gate. The inhibit function is controlled by the front panel RANGE MS switch. When the switch is set to the .1-.01 position, pin A is grounded and Q1 is permitted to follow the VFO signal. In all other switch positions, pin A is ungrounded, and Q1 is turned on, inhibiting the VFO output to the clock NOR gate. The clock NOR gate is described in the next paragraph.

4.3.1.4 Frequency Divider. See Figures 6-1, 6-2, and 6-3. The frequency divider consists of three decade counters, three divide-by-two counters, and associated gates, all arranged to divide the output of the VFO or crystal oscillator by a factor which will furnish shift pulses to the pseudorandom pattern generator at the data rate selected by the RANGE MS switch. All three decade counters consist of four flip-flop stages modified by feedback to provide a division by ten. The counter outputs are controlled by individual inhibit gates, as selected by the RANGE MS switch. Outputs from the inhibit gates are routed to the clock NOR gate.

Decade counter number 1 (Figure 6-2) consists of flip-flop stages Q12-Q13, Q14-Q15, Q16-Q17, and Q18-Q19. Its associated inhibit gate is Q11. This counter output is selected when the RANGE MS switch is in position 1-.1, CR1, or CR2. The input to the counter is supplied by oscillator NOR gate Q2. The counter output at Q16 is routed through CR18 and pin S to pin F of counter number 2 (Figure 6-1). Operation of inhibit gate Q11 is functionally identical to the operation of inhibit gate Q1. The inhibit gate output at pin L is routed to pin M of the clock NOR gate (Figure 6-3).

Decade counter number 2 (Figure 6-1) consits of flip-flop stages Q25-Q26, Q27-Q28, Q39-Q30, and Q31-Q32. Its associated inhibit gate is Q24. This counter output is selected when the RANGE MS switch is in the 10-1 position. The input to the counter is supplied at pin F by counter number 1. The counter output at Q29 is routed through CR18 and pin J to pin B of counter number 3 (Figure 6-3). Operation of inhibit gate Q24 is functionally identical to the operation of inhibit gates Q1 and Q11 (Figure 6-2). The inhibit gate output at pin C is routed to pin P of the clock NOR gate.

Decade counter number 3 (Figure 6-3) consists of flip-flop stages Q1-

Q2, Q3-Q4, Q5-Q6, and Q7-Q8. Its associated inhibit gate is Q20. This counter is selected when the RANGE MS switch is in the 100-10 position. The input to the counter is supplied at pin B. The counter output at Q8 is connected to inhibit gate Q20. Operation of Q20 is functionally identical to the operation of inhibit gates Q1-Q11 (Figure 6-2), and Q24 (Figure 6-1). The output of Q20 is connected to the clock NOR gate.

Transistor stage Q19 is a NOR gate which accepts clock signals from the four inhibit gates just described. A clock input from any inhibit gate turns on Q19. The resultant positive-going clock output at the collector of Q19 is coupled to flip-flop stage Q9-Q10.

Flip-flop stage Q9-Q10 divides the clock input by two and provides an output to two other divider stages. One output phase from the collector of Q9 is used to trigger divider stage Q13-Q14; the other output phase from the collector of Q10 is used to trigger divider stage Q11-Q12. These two dividers are the output stages of the frequency divider and provide timing signals for various internal purposes. The timing signals from the two dividers are 90 degrees out of phase with respect to each other.

Divider stage Q13-Q14 is the source of the main clock signal in the pattern generator. Because of the phase-locking process the main clock signal is maintained at a 90-degree phase lagging condition with respect to the incoming data. One output phase from the collector of Q13 is coupled through complementary emitter-follower Q15-Q16 to pin F. From pin F, the main clock signal is routed to contact A of the TX CLK switch, to pin 1 of the VFO phase-lock circuit (Figure 6-6), to pin D of RX TIMING switch in the receiver module, and to the SCTE level converter in the data set adapter.

The other main clock output phase from the collector of Q14 is inverted by Q21 and coupled through complementary emitter-follower Q22-Q23 to pin E. From pin E, the main clock signal is connected directly to the front panel SCTE connector.

Divider stage Q11-Q12 is the source of the quadrature (quad) clock signal in the pattern generator. Because of phase-locking process, the quad clock signal is maintained in phase (but inverted) with respect to the incoming data. The quad clock output at the collector of Q11 is coupled through complementary emitter-follower Q17-Q18 to pin N. From pin N, the quad clock signal is connected to the VFO phase-lock

circuit (pin 2, Figure 6-6), and to the crystal phase-lock circuit (pin A, Figure 6-1).

4.3.1.5 Pseudorandom Pattern Generator. See Figure 6-4, PC board NO345. The bit generator comprises an eleven-stage shift register, an Exclusive OR circuit, a feedback control gate, and a lock-up AND gate. Together, the four circuit elements form an m-sequence generator which provides a pseudorandom pattern of 2047 bits. The pseudorandom pattern is a binary sequence containing periods of relatively high cross-over density combined with comparatively idle periods of as many as ten consecutive marking and eleven consecutive spacing intervals (when referred to the pattern transmitted to the user).

(The expression "m-sequence" means that the output is a maximum-length linear shift register sequence. Different sequences are produced by changing register direct-feedback points in accordance with specified mathematical formulas. The pattern is called "pseudorandom" because it is not produced by a process which is truly random but by a process with a determined outcome which meets the requirements of certain statistical tests for randomness.)

The shift register portion of the bit-generator consists of flip-flop stages Q1-Q2 through Q21-Q22. The register may be timed either by the internal main clock pulses, or by external timing pulses (provided by a data set), as selected by the front panel TX CLK switch. The external clock signal, applied at the SCT input of either the pattern generator or the data set adapter, is shaped by external drive slicer Q9-Q10 and inverter Q20 (located on PC board NO347, Figure 6-2) and then connected to the TX CLK switch. The selected timing pulses are connected at pin S and coupled through driver stage Q23-Q24 to the shift bus of the register. The pattern output of the register is derived from the ninth and eleventh stages. Both complementary outputs of shift register stages 9 and 11 are presented to the Exclusive-OR gate consisting of transistor stages Q25 and Q26 by way of AND gates CR28-CR29 and CR33-CR34. The Exclusive-OR gate output at the collectors of Q25 and Q26 is the pattern generator output. This output is routed both to feedback control gate Q35 and to NOR gate Q27. From Q27, the complementary pattern output (inverted when compared to the Exclusive-OR output) is routed through level converter Q28 and complementary emitter-follower Q29-Q30 to both the data set adapter module and the SD connector. Level converter Q28, thus, converts positive logic "1" bits (5 volts) to negative logic "1" bits (-10 volts) causing the complement of the pattern generator output to be transmitted to the user.

Transistor stage Q35-Q36 forms a gate circuit which controls feedback to the first stage of the shift register. Inputs to the gate are from one of two sources: the pattern output of the Exclusive-OR gate, and the lock-up AND gate CR24-CR25. Normally, the input at R95 from the lock-up AND gate is at a low level, and Q35 and Q36 follow the output of the Exclusive-OR circuit in a complementary fashion. The output of Q35 and Q36 sets or resets the first stage of the shift register, Q1 and Q2, thereby providing the feedback which produces the 2047-bit pseudorandom pattern sequence.

The second possible input to the feedback control gate is from lock-up AND gate CR24-CR25. This AND gate functions to initiate the pattern sequence automatically in the event that the register is shifted into the forbidden state upon initial application of power. The forbidden state corresponds to the condition in which the shift register cannot sequence — hence the name lock-up. This occurs when all reset outputs of the shift register are in a high (reset) state. The condition is sensed by the lock-up AND gate in the following manner. When lock-up occurs, register stage Q2 is turned off and AND gate diode CR24 is back-biased. Simultaneously, the following register stages are also turned off: Q3, Q6, Q7, Q10, Q11, Q14, Q15, Q18, Q19, and Q22. Since the emitter circuits of Q3, Q6, ...Q22 are opened, error test gate Q32 (described in a later paragraph) is turned off and AND gate diode CR25 is back-biased. As a result, feedback control gate stage Q35 is turned on; the input gate to register stage Q1 is primed; and the following shift pulse turns off Q1 and turns on Q2. The changed state of the first stage then forward biases CR24, and feedback to the register is again provided by the Exclusive-OR output. The overall effect of this operation is to begin a new 2047-bit sequence.

4.3.1.6 Frame Pulse Circuit and Error Test Generator. See Figure 6-4. The frame pulse circuit consists of error test gate Q32 and emitter-follower Q31. This circuit provides a negative-going synchronizing pulse of one bit duration once per 2047-bit pattern frame. A frame pulse is generated each time register stages 2 through 11 are in the proper state to turn off error test gate Q32. When this event occurs, Q31 is turned on, and a negative-going pulse appears at the front-panel FRAME PULSE connector.

The error test generator consists of error test gate Q32, error test flip-flop Q33-Q34, error AND gate CR27-CR32, and the front-panel INSERT ERRORS-OFF-SINGLE switch. The error test generator provides either a single, unrepeated, frame error bit, or one error bit

per 2047-bit frame, as selected by the switch. Basically, the error test generator assumes control of output NOR gate Q27 for the time of the frame error bit. Control of this gate is normally held by the Exclusive-OR output at Q25-Q26. Thus, at the instant of error bit generation, the output of Q27 is inverted, and an error pulse appears in the output pattern.

When the INSERT ERRORS-OFF-SINGLE switch is in the OFF (center) position, the error test flip-flop is reset with Q34 on. This condition forward-biases diode CR32 and effectively grounds the junction of CR32-R120. As a result, control of output NOR gate Q27 is held by the Exclusive-OR circuit, and the normal output pattern is passed through inverter Q28 and complementary emitter-follower Q29-Q30 to the data set adapter module and SD connector.

When the INSERT ERRORS-OFF-SINGLE switch is in the SINGLE (down-momentary) position, the error test flip-flop is set with Q34 off. This condition back-biases AND gate diode CR32. The other AND gate diode, CR27, is also back-biased at the time of a frame pulse. As a result, the error test generator controls the output NOR gate with a positive-going pulse, and an inverted output appears at the SD connector. Each activation of the test switch to the SINGLE position will produce one error bit at the time of the next frame pulse. The error test flip-flop is reset, with Q34 on, by the trailing edge of the frame pulse applied through C28 to Q33.

When the INSERT ERRORS-OFF-SINGLE switch is in the INSERT ERRORS (up) position, the ground at pin 4 holds the collector of Q33 at ground, thereby holding the error test flip-flop set, with Q34 off. This condition produces the same results as the SINGLE position, except that an error bit will be generated automatically for every 2047-bit frame.

4.3.2 RECEIVER

The receiver module consists of the following items; a VFO phase-lock circuit, data and clock input shaping circuits, a receiver pseudo-random reference pattern generator, a delayed clock circuit, error detection circuits, and pattern synchronizing circuits. A detailed description of each item is presented in the following paragraphs.

4.3.2.1 AFC Phase-Lock Circuit. See Figure 6-6. The AFC phase-lock circuit includes a flip-flop (Q8-Q9) and an associated Exclusive-OR

circuit (CR5 through CR7, and Q10 through Q12). The phase-lock circuit measures the phase differences between the internal clock and the received data (crossover points), and then develops a control signal with a duty-cycle shift proportional to the difference. In addition, an integrator and associated amplifier convert the control signal variations to dc level variations suitable for operating a front-panel meter and a VFO driver.

The AFC phase-lock circuit is enabled or disabled by the front panel RX TIMING switch. When the switch is in the CLOCK position, the AFC enable gate, Q4, is clamped off (-12 volts) by the ground applied at pin 3, disabling the AFC tracking by the internal oscillator. Conversely, when the RX TIMING switch is in the DATA position, the grounded at pin 3 is removed, allowing Q4 to act as an inverter for the receive data from the data slicer. When the AFC circuit is enabled, phase-lock flip-flop Q8-Q9 is set (Q8 off) by pulses derived from the data slicer and applied to the base of Q8 through AFC enable gate Q4. Reset pulses derived from the quad clock input at pin 2 are applied to the base of Q9. Thus, the flip-flop is set by positive transitions of the data (RD) and reset by positive transitions of the quad clock, resulting in the waveform shown in Figure 4-3. Complementary outputs from Q8 and Q9 are applied to Q22 and to the phase-lock Exclusive-OR circuit. (The Q22 output is routed to the crystal phase-lock circuit.) Complementary transitions from the main clock input at pin 1 are also applied to the Exclusive-OR circuit to be compared with the outputs of Q8, Q9. Stage Q12 provides the inverted main clock for the Exclusive-OR function, and CR5, CR6, and CR7, Q12 form two 2-input AND gates whose outputs are inverted by Q10 and Q11 to form NAND functions. By applying true and complementary inputs to the NAND functions thus formed, the Exclusive-OR function is obtained. The output of the Q10, Q11 Exclusive-OR circuit, for the in-phase condition, is a combination of a squarewave at twice the clock rate and a squarewave at the main clock rate with an average fifty percent duty cycle. For a data-leading-internal-clock condition, the negative portion of the Exclusive-OR output becomes greater than the positive portion. Conversely, for a data-lagging-internal-clock condition, the negative portion of the Exclusive-OR output becomes lesser than the positive portion. Waveforms for the phase-lock sequence for in-phase, leading, and lagging conditions are shown in Figure 4-3.

Any shift in phase between internal and external signals produces a change in duty cycle at the output of the Exclusive-OR circuit. The change is integrated, and the resultant level is applied to differential

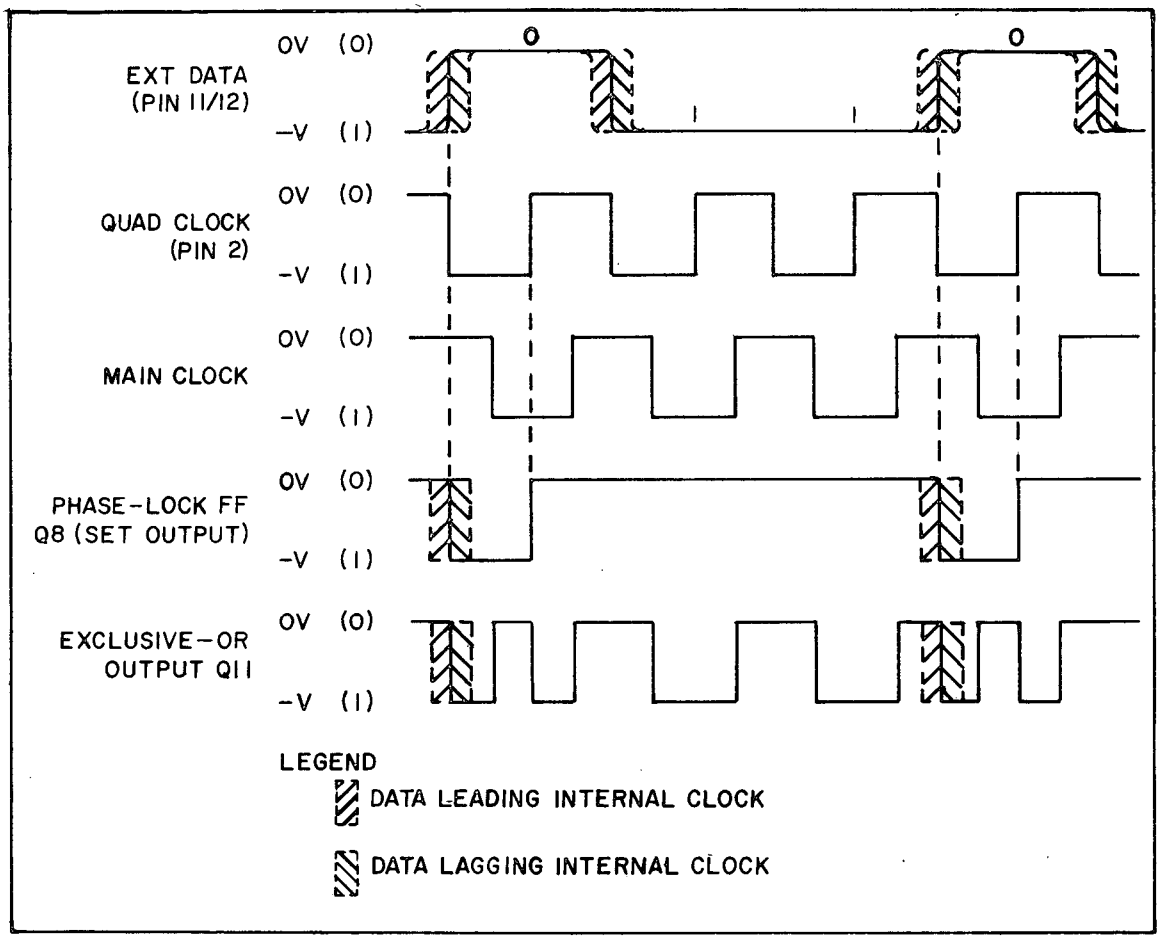


Figure 4-3. AFC Phase-Lock Sequence Waveforms

amplifier Q13-Q14. Different time constant values for the integration process are provided by the several positions of the VFO TIME CONSTANT switch. Position 1 provides the fastest phase tracking and thus is used with high-speed data. Position 2 is used with high- or medium-speed data. Position 3 is used with medium- or low-speed data. Position 4 is used with low-speed (teletypewriter rate) data.

The differential amplifier output at the collector of Q13 is further amplified by Q15 and passed through emitter followers Q17-Q16-Q18 to

pin D. From pin D, the output is routed by way of the OPR-CAL switch to the series 10-turn potentiometer and then to the VFO circuit, where it is used to control the frequency.

The front-panel meter on the receiver module visually indicates phase-lock. In operation, phase-lock is indicated by a smooth movement of the meter pointer over a wide range as the vernier dial is rocked back and forth through the indicated rate. Three internal adjustment potentiometers are associated with the meter circuit, namely; balance potentiometer R66, zero potentiometer R81, and frequency potentiometer R76. These potentiometers are adjusted during initial setup of the phase-lock circuit, as described in Section 5 of this manual.

The servo action of the phase-lock loop will attempt to hold the meter pointer at center scale: the condition where internal and external clocks are of the same frequency and phase, and where mid-bit sampling of the received pattern is achieved.

4.3.2.2 Data and Clock Input Circuits. See Figure 6-6. The data and clock input circuits include two slicer circuits, the front-panel RX TIMING switch, and an AFC enable gate. Since the two slicer circuits are functionally identical, only the data slicer is described in detail.

The received data pattern (the complement of the internally generated pattern) is normally applied to pin 12 of the receiver module from the data set adapter module. This data pattern is routed to the front panel DATA connector by way of pin 11 to allow monitoring of the data by external test equipment. Alternatively, a data pattern may be applied to the DATA connector, provided the pattern into the data set adapter module is disconnected. In either case, the pattern is then applied to transistor Q1 of the differential amplifier, Q1-Q2. The differential amplifier input circuit is designed to accept an NRZ signal with 0 volts equal to a space or logical "0" and -10 volts equal to a mark or logical "1." Rise and fall times are not critical, since the input circuit provides reshaping. The input impedance is a nominal 5000 ohms. Differential amplifier Q1-Q2 has a switching threshold of approximately -5 volts. Output signals from the collector of Q2 are connected to the base of Q3. The output of Q3 (the "true" pattern) is applied to AFC enable gate Q4 and to the receive pattern generator and error detection circuits.

The clock output from the data slicer is selected by the front-panel RX TIMING switch. When the switch is set to the DATA position, the AFC

enable gate Q4 is opened and the clock output at Q3 is passed to the phase-lock flip-flop. At the same time, the main clock output from the internal clock generator is selected by the switch for timing of the receiver pattern generator and error detection circuits. The data output at Q3 is routed to the error comparator circuit and the receive pattern generator feedback control circuit. When the RX TIMING switch is set to the CLOCK position, Q4 is blocked by a ground applied at pin 3, and an external clock signal clocks the receiver pattern generator and the error detection circuits.

The incoming clock signals are normally applied to the clock slicer from the data set adapter module by way of pin 9 of the receiver module. The CLOCK connector on the receiver front panel may be used to monitor the clock signal or, alternatively, may be used to apply a clock signal to the receiver module, provided that the clock input to the data set adapter module is disconnected. The incoming clock signal should be a squarewave varying between 0 and -10 volts. The transition from -10 to 0 volts should coincide with the transition from one bit to the next. This signal, after shaping by the clock slicer circuit, is applied to the clock inverter (Figure 6-7) and, subsequently, to the RX TIMING switch. The RX TIMING switch selects either the external clock signal from the clock inverter (Q3, Figure 6-7) or the internal clock signal from the main clock complementary emitter follower (Q15-Q16, Figure 6-3) and applies the selected signal to the positive-neutral level converter (Q2, Figure 6-7) which drives the receiver synchronizer and error detection circuits. The level converter accepts negative logic, in-phase clock signals (true during the second half of the data bit) and converts them to positive-logic, in-phase clock signals. Note, however, that when the internal (main) clock signal is used, this signal is offset by 90 degrees (one-fourth cycle) when compared to the incoming (RD) data.

4.3.2.3 Reference Pattern Generator. See Figure 6-7. The receiver pseudorandom pattern generator consists of 11-stage shift register A1 through A3-A, Exclusive-OR circuit A7-2 and A7-5, feedback control gate A7-11 and A7-14, and clock driver Q2 and A9-5. Together, the four circuits form an m-sequence generator which provides a pseudorandom pattern that is 2047 bits long, identical to the pattern generated in the pattern generator module.

The shift register is driven by way of A9-5 and A9-2 by signals from the internal clock or by external clock, as selected by the front panel RX TIMING switch.

During the pattern synchronization process, the "true" received data (RD) from the output of the positive-neutral level converter is clocked into the pattern generator. The pattern generator output (RP) is applied to the feedback control gate, A7-11, to the error comparator, and, through inverter A8-11, to the level converter, A13-2. The inverted reference pattern (RP) is then available at pin 5. The pattern generator feedback data is provided either by gate A7-11 or gate A7-14. During normal operation when the pattern is synchronized with the incoming data pattern, the true output of the resync flip-flop (A6-11) enables feedback control gate A7-11 which routes the register output back to the register input. At the register input (within A1) an inversion takes place to compensate for the inversion caused by the NAND gate, A7-11. The feedback data is then clocked into A1 of the register by the positive-going edge of the inverted clock from inverter A9-5 (see Figure 4-4). Since stages 9, 10, and 11 change states at the negative-going edge of the clock signal, a second inverter, A9-2, inverts the clock signal applied to these stages, causing them to shift at the same time as stages 1 through 8 (in A1). In this manner a perfect pattern is generated for subsequent comparison and error detection with the received data. When the internal pattern is out of synchronization with received data, the resync flip-flop enables feedback control gate A7-14 and disables gate A7-11. Gate A7-14 then routes the true received data (RD) from positive-neutral level converter Q1 to the register input and begins filling the register. When the resynchronizing circuits sense that the register pattern matches the received data, they reset the resync flip-flop, inverting the feedback control gates to return the generator to internal feedback operation. To ensure that the generator does not enter a locked (forbidden) state, the lock-up counter monitors the Exclusive-OR output of the generator. Since, under normal conditions, a maximum of ten bits can be zero at the Exclusive-OR output, the counter never reaches a count of twelve unless the pattern generator is in a locked state. This is true because the Exclusive-OR output is applied to the lockup counter reset input. The counter is then clocked by the CLK signal, advancing the counter until it is reset by a "1" from the Exclusive-OR. When the pattern generator is in the locked state, the counter advances to a count of twelve, causing "1's" at both inputs to NAND gate A16-14. The NAND gate output is then a "0" causing a "1" to be loaded into the first stage of the generator, ending the locked condition.

The outputs of register A2-A and A3-A are sampled by Exclusive-OR gate A7-2 and A7-5 to provide the 2047-bit pseudorandom register output. The true outputs of stages 9 and 11, A2-A and A3-A, are sampled

by NAND gate A7-2. (Register stages 9, 10, and 11 are connected so that the $\overline{Q}$ outputs (nomally the reset outputs) are connected to provide true data.) The output is applied to the error comparator circuit for comparison with the true received data.

4.3.2.4 Delayed Clock Generator. See Figure 6-7. The delayed clock generator consists of one-shot multivibrators A4 and A5, 2-input NAND gate A9-11, and J-K flip-flop A3-B.

Inverted receive clock pulses from A9-5 are applied to the A4 input, and inverted clock pulses from A9-2 are applied to the A5 input. Multivibrators A4 and A5 are triggered by the trailing edge of the clock pulses. The 7.5-kilohm resistor connected between pins 10 and 14 and the 390-picofarad capacitor connected between pins 10 and 11 of A4 and A5 are timing components which set the output pulse duration to 2 microseconds.

The outputs of A4 and A5 are negative going pulses which are time-displaced by one-half of a clock period. These pulses form the two inputs to NAND gate A9-11. The output of gate A9-11 is positive going pulses of 2-microseconds duration at twice the clock rate. These pulses are applied to pin 5 of J-K flip-flop A3-B. To ensure that the output of flip-flop A3-B starts in the proper state, the 2-microsecond pulse from one-shot multivibrator A4 is applied to the reset input, RD. At the positive-to-negative transition of the pulse, the flip-flop is reset. The positive-to-negative transition of the same pulse, after being inverted and slightly delayed by A9-11, toggles the flip-flop back to the set state. The next inverted pulse from multivibrator A5 then toggles the J-K flip-flop to reset state, and the following inverted pulse from A4 (by way of A9-11) sets the flip-flop. Thus, the output of the flip-flop is a negative-to-positive going signal, offset from the bit period by two microseconds. Since the output of A3-B changes state during the negative going transition of each input pulse, the output pulses have the same pulse repetition rate as the receive clock signal, but delayed by approximately 2 microseconds from the clock.

4.3.2.5 Error Detection Circuits. See Figure 6-7. The error detection circuits consists of error comparator A8-5 and A8-14, error gate A10-2, and error flip-flop A10-11 and A10-14.

Input signals to the error comparator circuit consist of the external pattern from positive-neutral level converter Q1 and the internal pattern from the reference pattern generator. The external and internal

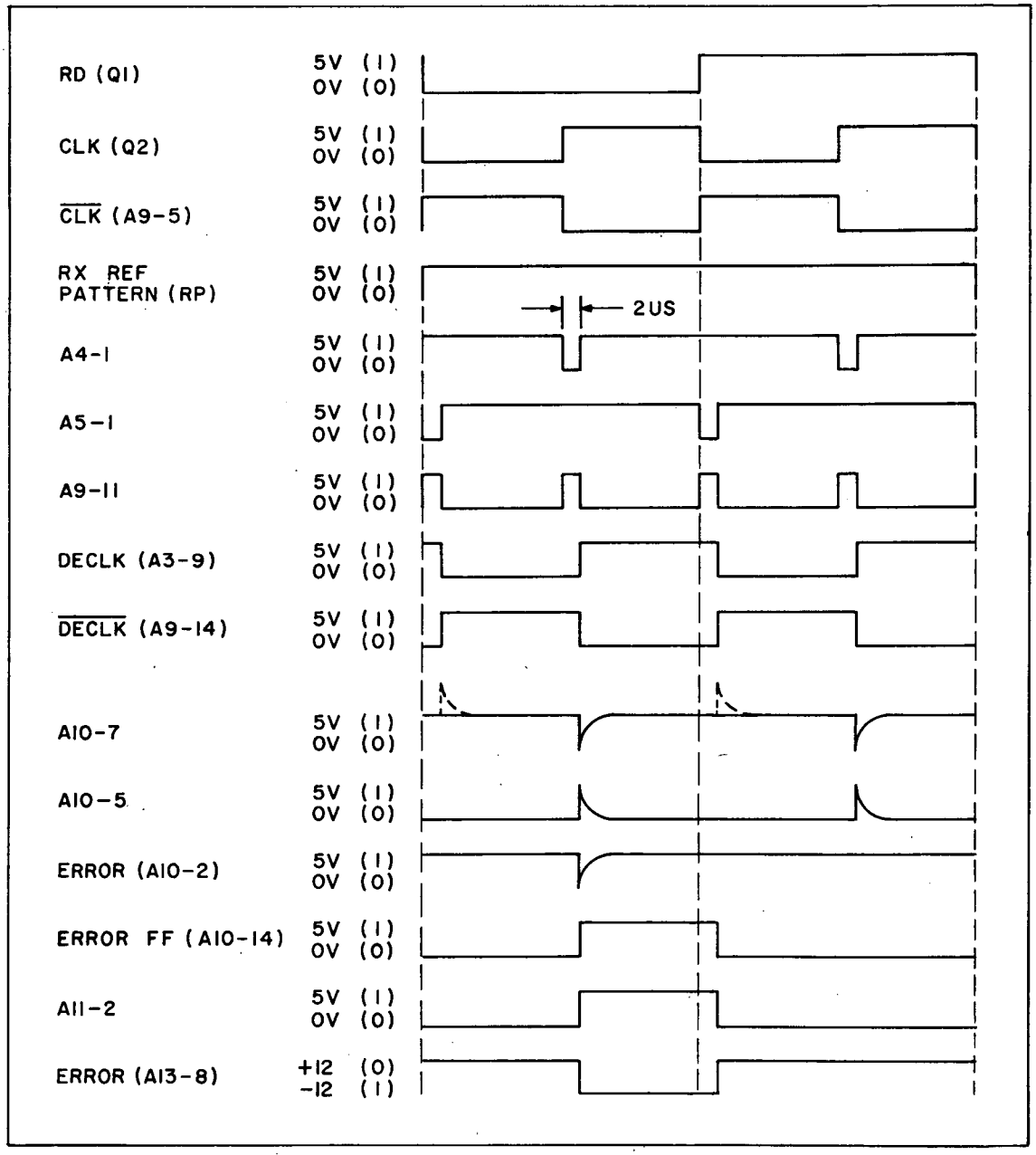


Figure 4-4. Synchronizer and Error Detection Circuit Timing Diagram (One bit in error)

patterns of the same polarity are simultaneously applied to gate A8-5. The patterns are inverted by A8-2 and A8-11, and simultaneously applied to gate A8-14. As long as the two patterns are synchronized and the input bits are in agreement, either A8-5 or A8-14 will be enabled thereby providing a low level at the output of the comparator (an Exclusive-OR circuit). If a disagreement occurs, both gates will be disabled, thereby providing a high level at the output of the comparator.

The comparator output provides one of the two inputs to error gate A10-2. The other input is supplied by the sample pulse generator. If the received and internal patterns are in agreement at sample time, the comparator output is low and the error flip-flop is not set. If the patterns disagree, the comparator output is high and the error flip-flop is set by the negative-going pulse from A10-2. Since the sample pulse occurs once each bit time, the two patterns are compared on a bit by bit basis and thus provide real-time error detection of the input pattern. The error flip-flop is reset by the next negative-going receive clock pulse, delayed 2.0 microseconds by the delayed clock generator. The flip-flop output provides one input to error inhibit gate A11-2. The other input is provided by resync flip-flop A6-11 and A6-14. When the resync flip-flop is reset, its input to the error inhibt gate is high, and the gate is enabled. Bit errors sensed by the error flip-flop are thus passed to the error counter module through inverter A11-14 and negative-neutral level converter A13-6, which converts a 0-volt input to a 0-volt output and a +5-volt input to a -12-volt output (positive logic true to negative logic true), providing a NOT errors signal at the error counter module. A bi-polar logic level output is supplied from gate A11-2 to terminal 5 of TB1 on the rear panel, and the ERROR PULSE connector on the front panel by way of bipolar level converter A13-C, which converts a 0-volt input to a +12-volt output and a +5-volt input to a -12-volt output (positive logic true to negative logic true), providing "true" errors at the connector and terminal board. The error flip-flop output is also used to reset the 16-unit counter in the pattern synchronizing circuits.

4.3.2.6 Pattern Synchronizing Circuits. See Figure 6-7. The pattern synchronizing circuits consist of the front panel AUTO-MAN-RESYNC switch, resync flip-flop A6-11 and A6-14, 16-unit sync counter A14, decoder gate A12, and counter advance gate A11-B. Pattern synchronization is initially established by opening the internal feedback loop of the reference pattern generator and inserting external data until 16 good bits are received in succession. At that time, the internal feedback loop is closed, and the pattern generator continues to produce a

perfect pattern.

When the two patterns are synchronized, the resync flip-flop is reset by the sync counter and prevents the 16-unit sync counter from operating.

The resync flip-flop can be set by a negative going pulse at A6 pin 12 in either of two ways. When the RESYNC switch is depressed, a ground at pin 11 causes a single negative going pulse at the output of the resistor-capacitor network C3-C4, R7-R8. When the RESYNC switch is in the AUTO position, a ground at pin 7 is inverted by A6-5 to enable the auto resync NAND gate A6-2, which then allows positive-going resync commands from the resync recognition circuits in the error counter module (ECM) to set the resync flip-flop. The resync flip-flop, in turn, enables the external data feedback gate, A7-14, in the reference pattern generator, disables the error inhibit gate, A11-2, enables the 16-unit sync counter, A14, and lights the front-panel SYNC ALARM indicator. In addition, the output of the resync flip-flop is inverted by A12-2, providing a NOT resync signal (+5 to 0 volts) to the ECM. The sync counter is then advanced by gate A11-5 each time the internal and external patterns agree. Pattern agreement is detected by sampling the error gate output, A10-2, with the sample pulse. The error gate output is high if no error is detected and, consequently, counter advance gate A11-5 is enabled. If an error is detected, the sync counter is reset by the error flip-flop, so that 16 consecutive good bits must be detected.

In operation, the external pattern is inserted into the reference pattern generator shift register until the external and internal patterns are the same. At that time, the sync counter is advanced 16 consecutive times, causing the output of decoder gate A12 to go low. Resistor-capacitor network R14, C5 differentiates the level change, producing a negative going pulse at A6 pin 9 to reset the resync flip-flop. The flip-flop then returns the shift register to internal feedback, enables the error inhibit gate A11-2, and turns off the SYNC ALARM indicator. The MAN position of the RESYNC switch is simply an off position which disables automatic resynchronization.

4.3.2.7 Voltage Regulator Circuit. A voltage regulator circuit, consisting of Q6 and associated components, converts the +12 volt input to the synchronizer and error detector circuits to a regulated +5 volt output required by the logic components used.

4.3.3 ERROR COUNTER MODULE

The error counter module consists of a translator board, a recognizer board, a channel outage indicator board, a counter display control board, three counter display boards, and a power supply board. A detailed circuit description of each board is presented in the following paragraphs.

4.3.3.1 Translator Board. See Figure 6-10. The input translators consist of saturated transistor logic level shifters. The translators for the selected receive clock, NOT delayed clock, and NOT receiver reference pattern inputs are essentially identical using 2N4124 transistors (Q411, Q412, and Q413) in a saturated configuration. The diodes in that configuration (CR401, CR402, and CR403) serve as clamps to protect the switching transistors. Each transistor feeds an integrated circuit inverter to provide the drive capability for the next stages. These three translators give a logical "1" (+5 vdc) output for a 0-volt logical "0" input from the receiver module, thus converting a negative logic "false" signal to a position logic "true" signal (and vice versa).

The bit-errors translator is different from the other input translators in that it is designed to yield an adjustable voltage level of error pulses in addition to the +5-volt swing outputs. Transistor Q406 is a field effect transistor in a constant-current configuration to yield a defined current through potentiometer R440 and, thus, a definable, constant voltage level for outage errors. The resistive divider is designed so that with the FET turned on, (input at -10 volts), Q408 will be reversed biased by approximately one volt, and its output will be +5 volts, providing a NOT bit error output at the collector. With a logical "0" (0 volt) error signal, the FET is turned off; Q408 is forward biased; and its collector is 0 volt. The opposite sense of the error pulse is provided by way of IC401.

The resync input translator, Q410, responds to a 5-volt swing (+5 to 0 volts) from the resync flip-flop in the receiver module. A 0-volt input (resync) will cause Q410 to cutoff, giving a "true" logical "1" output. Low sense of the resync flip-flop signal is provided by gate 401-11.

The output translators consists of five output drivers, Q401 through Q405, and a resync command interface, Q409, to the receiver module. The output drivers give a -12-volt logical "1" output for a +5-volt logical "1" input. Filter capacitors C401, C403, C405, C404, and C407 on the driver outputs limit switching time to approximately one micro-

second. Two 470-ohm resistors are placed on the output circuit of each driver so that a short-circuit on the output line will not impair operation of the error counter module. The resync command translator (Q409) inverts the negative input pulse (+5 to 0 volts) from the resync command circuit on the translator board and shifts the input logic level from 0 and +5 volts to +12 and 0 volts, respectively.

4.3.3.2 Recognizer Board. See Figure 6-11. The received data is reconstructed by shifting the Exclusive-OR output of the error pulse signal (IC618, pin 3) and the receive reference pattern into the predictor. This insures that the predictor interprets each data bit in the same way as the receiver does. Since the pattern signal from the receiver module is changing when the predictor is clocked by the CLK signal, the pattern is delayed by flip-flop DP (IC619, pin 8) and made coincident with the delayed clock (DECLK) and the error pulses to avoid a race through the level-shifters.

The output of the predictor consists of an error signal, LPE (IC623, pins 8 and 9), with a duration of a full bit-time. This signal resets the bit counter (IC624 and IC625) and error flip-flop, EH (IC629, pin 2) of the 100-bit system. It also enters a logical "1" into the master section of the all-"1" detecting flip-flop, NZ (IC629, pin 7), if the current bit is a "1". When the bit counter reaches 89, this flip-flop will be clocked. Although both the J and K inputs will be low, the master section will still remember this logical "1" if all "1's" have persisted for 100 bits and prevented activation of the direct reset input. If this is not the case and EH has continued to be clocked since the last predictor error, a resync command is issued coincident with the positive going transition of the DECLK signal. The resync pulse is reissued until the direct-set input of LPE is activated to reset the 100-bit system. If the received data is not corrputed by noise, the bit counter will recycle every 100 bits until an error occurs, which generates a predictor error and resets the system in preparation for detecting a slip-sync. Operation is similar for a received pattern of all "1's," except that NZ remains on until the first "0" occurs.

The 2000-bit system is completely reset by the resync flip-flop, the NZ flip-flop (100-bit loop) or the RIC flip-flop (IC626, pin 8) in the all-"1" and repeating "1000" detectors. After the reset signal disappears, the error pulse counter (IC615-IC617) increments on the trailing edge of the error pulses. A clock signal is added with LPE to produce pulses (IC611, pin 3) for the predictor error counter (2000-bit loop, decision circuit). After 250 bits, the edge-catcher, EOT (IC623) (in the test

length counter), produces a pulse if less than 100 error pulses have been counted. This pulse resets the test-length (IC620-IC622), error pulse, and predictor error counters (IC613-IC615) (error pulse and predictor error counters), returning the system to its initial state. If 100 or more errors have been counted, the flip-flop $\overline{Z}$ (IC602, pin 3) of the up/down counter is set, preventing the EOT flip-flop from setting until the test have run for 1750 bits. This pulse resets the counters as before, but the overflow bits, ER (IC603, pin 5), flip-flop and the NP flip-flop (IC603, pin 9) are not clocked off until the trailing edge. While this pulse is present, a resync command (IC628, pin 8) is issued if the error pulse counter has overflowed and the predictor error counter has not. If neither has overflowed, the trailing edge of the EOT signal resets the up/down Y and $\overline{Z}$ flip-flops (IC602), returning the system to its initial state.

If the predictor error counter has overflowed, the Y and $\overline{Z}$ flip-flops are clocked to a "10" condition which causes another 1750-bit test regardless of the error rate in the first 250 bits. A second failure of the pseudorandomness test will clock the Y and $\overline{Z}$ flip-flops to a "1, 1" state, and subsequent failures will cause them to remain in that state until a test is passed. As long as the Y signal remains a "1", the system is inhibited from issuing a resync command. If two consecutive tests are passed, the Y-$\overline{Z}$ flip-flops will count down to "1, 0" and then to "0, 0," returning the system to its initial state.

The repeating "1000" detector uses a pair of flip-flops, A and B (IC606), which remain in the "1, 1" state with an input of all "1's" and in the "1, 1" state when receiving all "0's." These flip-flops automatically synchronize with the idle code when it begins, and then count in Gray code as long as the code persists uncorrupted by noise. Every fourth data bit is inverted by the Exclusive-OR gate (IC618, pin 6) to provide a reset signal for the 4-bit binary counter (IC608). The counter is clocked by the negative transition of flip-flop A, incrementing every four bits until the code is broken. The counter overflows after the code has persisted for 63 bits, setting flip-flop RIC (IC626, pin 8). This inhibits resync commands and causes reset pulses RP (IC627, pin 3) which set EOT, aborting any tests in progress and holding the 2000-bit system in its initial state until a break in the idle code resets RIC.

4.3.3.3 Channel Outage Indicator Board. See Figure 6-12. The channel outage indicator circuitry consists of four sections; the error integrator, the 10-second timer-integrator reset, the alarm trigger circuitry, and the lamp drivers and latching alarm.

The error integrator consists of R523, C504, Q503, and R517. The integrator is the standard circuit configuration of a Miller integrator. In operation, as outage error pulses introduce step functions into C504, the voltage level at the base of Q502 increases until it reaches its defined trigger voltage of approximately 4.9 volts. At that time, Q502 is turned on, thus cutting off Q507 by reverse-biasing the base-emitter junction. This forms the D input to IC502, pin 2 (0 vdc, logical "0"). When this occurs, the time-average-error-rate is less than the set fixed level (nominally, 25 percent).

During this period, the timer functions to reset the integrator after a specified time (nominally 10 seconds). The timer configuration is a unijunction, relaxation oscillator which is operated about its temperature stable point. Capacitor C505 charges through R525 until the emitter of Q506 reaches a trigger level which is determined by the unijunction's intrinsic stand-off ratio. At this point, base 2 of Q506 goes low as the unijunction fires, turning on Q504. This causes the gate of Q508 to go to 0 volt, turning on the FET and resetting the integrator by discharging C504. The reset pulse is held until capacitor C506 charges toward -12 volts through R526 and R511.

The unlatched version of the alarm (IC502) is clocked by way of Q505 and IC503, pin 8, at the end of each sample period, to represent the state of the channel from one period to the next period. The latched version of the alarm is composed of an R-S configuration of IC501, serving as both a latch and a lamp driver.

The three lamp drivers are essentially identical. Each uses a type MC858P quad, two-input power gate to drive the display indicator lamps and to form half of the latching R-S flip-flops. Dark current resistors, R506, R503, and R509 are provided to prevent current surges from damaging the driver logic during lamp turn-on. The audible channel outage alarm uses three dark current resistors, R503, R502 and R501; the latter two provide the biasing for Q501. Q501 is the switching element for controlling the buzzer, and is disabled by removing its ground supply to its emitter by means of S708.

The adjustments necessary for proper operation of the channel outage indicator board are R525, which determines the time constant for firing of Q506, and R440 on the translator board (see Figure 6-10), which determines the voltage level of the outage errors input signal being received by the errors integrator. The procedure for adjusting the components is described in Section 5.

4.3.3.4 Counter Display Control Board. See Figure 6-13. The counter display control board consists of the display mode control, block length detector, error block enable, and counter control circuits.

The display mode control consists of an enable switch (S301) which allows either pin 13 of IC306, in the continuous mode, or pin 10 of IC306, in the auto inhibit mode, to be enabled by pull-up resistors R301 and R302. In the auto inhibit mode, pin 8 of IC306 goes low when a "true" resync signal indicates that the receiver pattern generator is in the resync condition. The "false" output disables IC307 and IC306 at pins 2 and 4 respectively, thus, inhibiting bit errors and clock pulses from reaching the error block enable and block length detector.

In the continuous mode, during a resync condition, pin 11 of IC306 goes to a "0" to disable IC307 at pin 1 and to introduce an artificial 50 percent error rate by means of the D flip-flop (IC310). The D flip-flop consists of a trigger flip-flop configuration with $\overline{Q}$ returned to the D input. Under normal operating conditions, when the received and internal patterns are in synchronism, bit-errors and clock pulses are enabled through to the error block enable and block length detector.

The block length detector is a series of four decade counters (IC301 through IC304) in a "ripple-through" configuration, triggering from incoming clock pulses (CLK). This configuration is used in conjunction with four BCD thumbwheel switch assemblies (S701 through S704). When a switch is set to a specific number, the decoupling diodes are forward biased and hold pin 1 of IC308 at 0.6 volt (logical "0"). When the selected number is reached, all the diodes are reversed biased and pin 1 of IC308 goes high causing its output pin 2 to go low, setting the R-S flip-flop and causing the outputs 4 and 6 of IC308 to go high, resetting all of the decade counters to "0", and terminating the high condition at pin 1 of IC308.

Pin 8 of IC311 goes high as the R-S flip-flop is set, which enables pin 1 of IC312, and enables the next clock pulse to be fed to the counter control, IC309 pin 2, through the inverter, IC309 pins 4 and 5. This configuration ensures a pulse duration of a minimum of 5 microseconds (clock at 100 kHz), and a maximum of one-half bit time. On the leading edge of the output pulse, the edge detector is triggered, placing a "0" output on pin 6 of IC312 and resetting both R-S flip-flop configurations of IC311.

The error block enable circuit is designed so that the number selected

on the thumbwheel switch (S705) is the number of errors permitted per block. Decade counter, IC305, triggers on the trailing edge of the bit-error pulse. Until the number specified by the switch setting is reached, CR309 is forward biased due to a low condition of the clock, holding pin 8 of IC308 high at pin 9. If another error is detected, the output of pin 8 goes to a "0" on the leading edge of the bit-error which represents one more error than is permitted per block. The "0" output of pin 8 sets the R-S flip-flop configuration enabling the IC307 output (pin 6) at input pin 5 to respond to the output clock pulse when the block has been detected (enabled by the block length detector at pin 4).

The counter control circuit is formed by three, two input gates, which are enabled by the RUN-STOP-RESET switch when in the RUN position. At this time, a +5-volt level is applied to input pins 1, 9, and 13 of IC309, to enable the outputs to the three counter display boards. In the STOP position a pull-down resistor, R303, is used to insure that the counter control enable circuit will not go above logical "0."

4.3.3.5 Counter Display Boards. See Figure 6-14. Three counter display boards contained in the error counter module are used to display bit errors, block errors, and blocks counts. Each counter display circuit consists of six type N7490A decade counters (IC101 through IC106) arranged as a six decade ripple-through counter. Each counter contains decoder/drivers (IC107 through IC112) and readout tubes (DS101 through DS106). Reset-to-zero of all counters is accomplished by a logical "1" (+5 volt) level change applied to pins 2 and 3 of each counter; reset-to-nine of each counter is disabled by grounding pins 6 and 7.

The overflow circuitry consists of a trailing edge detector implemented with a resistive divider, R107 and R108, to insure worst case logical "1" (approximately 2.5 volts) operation from the coupling capacitor C101. This circuitry gives a negative transition pulse of approximately 10 microseconds on the trailing edge of the most significant 8-bit at pin 11 of IC101. The output is then fed to diode CR101 and, in parallel, to the trailing edge detector of the other two counter display boards. These signals then feed an inverter.

Clock pulses are applied at pin 14 of IC106 for either the bit errors, the block errors, or the blocks counter display board. The type N7490A counter functions in the decade count mode by clocking pin 1 (C_B) from the 1-bit (pin 12) of each counter.

High voltage (+200 vdc) is supplied to each of the six display tube anode resistors (R101 through R106) to yield the nominal operating current of 1.35 ma for each tube. Each decoder/driver, type N7441B, receives the 8-4-2-1 BCD code from the counters and decodes it to ten-line logical "0" outputs. The function of the driver is to allow any given cathode to "float" at approximately 50 to 60 vdc until its specific coded input is enabled. At this point, the appropriate cathode is grounded through the decoder/driver to the high voltage ground (HV GND), thus lighting a specific numeral. A separate HV GND return is used to reduce noise introduced into the ground line.

Two bypass capacitors, C102 and C103, are placed on the +5-volt supply to the counters and decoder/drivers to reduce noise due to TTL current surges.

4.3.3.6 Power Supply Board. See Figure 6-9. The low voltage regulator is a series regulator, consisting of three functional blocks. The first is the reference block which is composed of a field effect transistor, Q210, operated as a current source at its zero temperature coefficient point. The second block consists of the voltage amplifiers, Q203 and Q204, in a differential-pair configuration, with associated drivers Q202 and Q205, for the pass element. The final block consists of the pass element, Q701, which is a type 2N3055 power transistor mounted on the rear chassis (see Figure 6-34). Its associated driver, Q201, is mounted on the power supply board.

The low voltage regulator employs an "off-board" voltage level sensor (LEVSEN) to provide the correct voltage at the main feed point on the module chassis. Shunt resistor R212 and transistor Q209 provide current limiting at approximately 2.6 amperes.

CAUTION

The high voltage regulator is NOT designed to sustain a short circuit condition. Inadvertent grounding of the +200 volt supply may cause damage to this power supply.

The high voltage regulator consists of three functional blocks. The first is a high voltage transistor, Q206, operated in a current generator mode which is split between the pass transistor, Q208, and a standard voltage amplifier, Q207.

4.3.4 POWER SUPPLY MODULE

See Figure 6-16. The power supply module consists of four individual rectifier sections which provide the following outputs; a full-wave filtered +12 volts, a full-wave filtered -12 volts, a full-wave filtered +15 volts, and a half-wave unfiltered -12 volts. All four supply voltages are derived from a single, center-tapped secondary winding of power transformer T1. Primary ac power is applied to the module by means of the front panel POWER ON switch, S1. Fuse F1 protects the supply from overload. POWER indicator lamp DS1 is connected directly across one side of the transformer secondary, and glows to indicate that power is turned on.

4.3.5 DATA SET ADAPTER

See Figures 6-17 an 6-18. The data set adapter consists of receive and send level converters for voltage driven and current driven data sets, lamp drivers, clamps, BNC connectors, and front panel switches to select the transmitted pattern and interface levels. The electronic circuits are located on two functionally identical printed circuit boards. Each board contains two receive level converters, one send level converter, and two lamp drivers.

4.3.5.1 Receive Level Converters — Voltage Interface. Three receive level converters are used with voltage interface data sets: one level converter connected to J1, and two level converters connected to J2. The converter circuits are designated as follows: receive data (RD) circuit, serial clock receive (SCR) circuit, and serial clock transmit (SCT) circuit. Since the three circuits are functionally identical, only the receive data circuit is described.

The receive data circuit consists of level converter stages Q1 through Q6. Stages Q1 and Q4 function to provide the proper input impedance and switching level, respectively, for differential amplifier Q2-Q3. Stages Q5 and Q6 provide the converted output level. In operation, when the front panel INTERFACE selector switch, S3, is set to the E position, a -12-volt control level at PC board pin E turns off Q1 and Q4. Turning off Q1 adjusts the input impedance of Q2 for a +6/-6 volt input at pin A. Turning off Q4 provides the differential amplifier with a switching level of approximately +2 volts at the base of Q2. As a result, when +6 volts is applied to pin A, Q2 is turned on and Q3 is turned off. The collector output of Q3 then causes Q5 and Q6 to turn on, and the output at pin B is clamped at zero level.

When -6 volts is applied to pin A, Q2 is turned off and Q3 is turned on. The collector output of Q3 then causes Q5 and Q6 to turn off, and the output at pin B is raised to -10 volts.

4.3.5.2 Receive Level Converters — Current Interface. The same three receive level converters used with voltage interface data sets are used with current interface data sets. Circuit characteristics, however, are slightly changed because a different control voltage is used. The circuit description is again directed to the receive data circuit.

When the front panel INTERFACE switch is set to the I position, a +12-volt control level applied to PC board pin E turns on Q1 and Q4. Turning on Q1 terminates the input at pin A with 100 ohms (R5). Turning on Q4 clamps the junction of resistors R11 and R12 to zero level, thereby providing the differential amplifier Q2-Q3 with a switching level of approximately +1 volt. Input signals less than 5 ma or greater than 23 ma into 100 ohms are then varied around the +1-volt level. An input signal less than 5 ma produces a -10-volt output at pin B, and an input signal greater than 23 ma produces a zero-level output.

4.3.5.3 Send Level Converter — Voltage Interface. Two send level converters are used with voltage driven data sets, one on each printed circuit board. The converter circuits are designated the send data (SD) circuit and the serial clock transmit external (SCTE) circuit. Since the two circuits are functionally identical, only the send data circuit is described.

The send data circuit consists of level converter stages Q14 through Q16, and complementary emitter-follower driver stage Q17-Q18. In operation, when the front panel INTERFACE switch is set to the E position, a -12-volt control level applied to the base of Q14 through R53 turns off Q14. This action allows voltage divider R59-R60 to supply a negative voltage to the bases of Q17 and Q18 whenever Q15 is turned off. Circuit conditions for Q15 are determined by the input levels at PC board pin K, as selected by the front panel MODE switch, S4.

The front panel MODE switch has three positions labeled PR, 0, and 1. The PR position selects pseudorandom data at 10 to 100,000 bps from the pattern generator module. The 0 and 1 positions place +6- and -6-volt levels, respectively, on the send data line of voltage driven data sets. When the INTERFACE switch is set to the I position (to interface with current driven data sets), the 0 and 1 positions produce output currents greater than 23 man and less than 5 ma, respectively, and

the rise/fall time of the output signal is limited 0.3 microseconds by an inductor in series with the output. When the INTERFACE switch is in the E position, a capacitor is added in parallel with the output, limiting the rise/fall time of the data or clock signal to 6 microseconds.

When the input level at pin K is -10 volts, Q16 is turned off, thereby causing the base voltage of Q15 to rise to +12 volts. This action turns Q15 off and allows the base of Q17 to go to approximately -8 volts. The same voltage is then available at pin L. When the input level at pin K is 0 volts, Q16 is turned on and the base of Q15 is driven negative with respect to its emitter. This action turns on Q15 and allows the base of Q18 to go to approximately +8 volts. The same voltage is then available at pin L.

4.3.5.4 Send Level Converters — Current Interface. The same two send level converters used with voltage driven data sets are used with current driven data sets. Circuit characteristics, however, are slightly changed because a different control voltage is used. The circuit description is again directed to the send data circuit.

When the front panel INTERFACE switch is set to the I position, a +12-volt control level applied at PC board pin D turns on Q14. This action clamps the junction of R59 and R60 to a zero level. As a result, 0 and -10 volt inputs at pin K are converted to currents at pin L greater than 23 ma and less than 5 ma, respectively, into 100 ohms. An inductor in series with the output limits the rise/fall time of the output current.

4.3.5.5 Indicator Lamp Driver. Four indicator lamp drivers, two on each printed circuit board, are included in the data set adapter module. All four lamp drivers are used in both the voltage and the current interface mode. The driven indicator lamps are designated CS (clear to send), DSR (data set ready), COO (carrier on-off), and SQ (signal quality). Since the circuits are functionally identical, only the CS circuit is described.

The CS lamp driver circuit consists of transistor stages Q19 and Q20. Input levels are applied at PC board pin M. Switching of input level for operation on voltage or current interface mode is not required, since the circuit will accept either +6/-6 volt levels or currents less than 5 ma and greater than 23 ma. A +6-volt or 23-ma input turns on emitter-follower Q19. This action forward-biases Q20 causing it to conduct, thus completing the ground return circuit of the front panel CS lamp, connected at pin P through the current limiting resistor, R44, causing

the lamp to light. When Q20 is off, R45 provides a 470-ohm ground return path across Q20, providing idle current for the CS lamp.

4.3.5.6 Request to Send Circuit. See Figure 6-18. The request-to-send circuit consists of front panel RS switch S2, and associated resistor R1 on printed circuit board NO355. This circuit functions to supply a signal level to the data set to enable it to transmit data. In the ON position, the RS switch supplies a request-to-send signal to the selected data set. The request-to-send signal is a positive voltage for voltage driven data sets, and a current in excess of 23 ma for current driven data sets. (The data set acknowledges receipt of the request-to-send signal by returning a clear-to-send (CS) signal to the data set adapter module.) In the OFF position, the RS switch supplies either a negative voltage to a voltage driven data set or a current less than 5 ma to a current driven data set to inhibit transmission of data.

4.3.5.7 BNC Connectors. Five BNC connectors are provided on the data set adapter front panel. These connectors are wired in parallel with signal connections on connector J7 at the rear of the chassis and provide convenient monitoring points for signals going to or coming from the data set. When the multiple connector (J7) at the rear chassis is not used, the BNC connectors may be used to interface with the equipment to be tested.

SECTION 5

MAINTENANCE

5.1 GENERAL

This section contains information concerning maintenance of the Model 600F Data Transmission Test Set, and parts lists for items that may require replacement due to wear, deterioration, mechanical breakage, or burnout.

The maintenance information is intended to assist assigned personnel in keeping the Model 600F in proper operating condition. Both preventive maintenance, which includes a schedule of general inspection procedures and cleaning, and corrective maintenance which includes alignment procedures and troubleshooting procedures are given. Although some preventive maintenance will normally be performed by the operator, all corrective maintenance should be performed by a qualified technician who should have a thorough understanding of the Model 600F circuit theory.

WARNING

The Model 600F with the Model 1225 Error Counter Module operates from a 120-vac power source and employs other high voltages. These voltages are always dangerous to life. Use extreme caution when working on the equipment.

5.2 PREVENTIVE MAINTENANCE

Routine inspection and cleaning as described in the following paragraphs should be performed on the Model 600F to detect potential malfunctions and to prevent failures which will degrade performance of the equipment.

5.2.1 INSPECTION

A general component inspection procedure is shown in Table 5-1. Regularly scheduled inspections using Table 5-1 will assist personnel in detecting potential troubles and correcting them before operational failures occur. A semi-annual inspection is normally sufficient. More frequent inspections may be necessary, however, if the equipment is located in a poor environment or is otherwise harshly treated.

Table 5-1

GENERAL INSPECTION PROCEDURES

Component	Condition	Cause	Correction
Resistors	Discolored, swollen or cracked	Overheated	Correct overload condition and replace defective resistors
Capacitors	Leakage, bulging, split case, or broken end seals	Physical damage or dielectric breakdown	Replace defective capacitor
Transformers and inductors	Discolored insulation or windings, leakage	Overloaded, physical damage	Check circuit for possible cause and replace defective part
Connectors and jacks	Bent pins, charred insulation, marred threads, moisture, dirt, or grease	Improper handling	Straighten pins, clean or replace part
Switches and controls	Broken, worn, bent or dirty	Rough handling, normal wear	Clean, straighten or replace
Indicator lamps	Broken or burnt out	Rough handling, excessive current	If broken, replace; if burnt out, check circuit for possible cause. Correct cause of burnt-out lamp and replace lamp
Wiring and cables	Cut or frayed insulation, broken wires or connections	Improper handling	Repair or replace
Solder connections	Loose or corroded connections, cold solder joints	Improper soldering	Clean and resolder

5.2.2 CLEANING

The Model 600F should be kept dry and free of dirt, grease, and oil. Any regularly scheduled cleaning routine should include the removal of dust from both the equipment exterior and interior. Avoid using sharp-edged cleaning tools, which can scratch surfaces and damage printed-circuit boards. Instead, use a soft brush or rag to prevent dirt build-up and possible short circuits. The equipment exterior should be cleaned at least once a month; the interior may be cleaned on a quarterly basis, or more frequently, if necessary.

5.3 CORRECTIVE MAINTENANCE

Corrective maintenance procedures generally involve visual observation of operating conditions to localize the cause of malfunction to a specific area. The following corrective maintenance information will provide the service technician with a systematic procedure for locating and repairing equipment troubles. Table 5-2 is a list of the required test equipment. Test equipment with equivalent characteristics may be used in place of recommended equipment.

Table 5-2

REQUIRED TEST EQUIPMENT

Test Equipment	Recommended Model	Manufacturer
Oscilloscope (Dual Trace)	535A	Tektronix
Frequency Counter	6C46	Atec, Inc.
Multimeter	80	Weston
Squarewave Generator	211B	Hewlett-Packard

Table 5-3 is a troubleshooting chart which will aid the service technician in isolating troubles to a specific area. This table uses the familiar "symptom, probable cause, and remedy" method of approach. If spare printed circuit boards are available, troubles can be quickly isolated by substituting boards. The several waveform charts found in Section 3 will help in locating the defective circuit or component. In addition, the schematic diagrams in Section 6 should be used during troubleshooting operations.

C-2

Table 5-3

SYSTEM TROUBLESHOOTING CHART

Symptom	Probable Cause	Remedy
Primary POWER lamp does not light	1. Power cord not plugged in 2. Blown F1 fuse 3. Defective lamp 4. Defective module	1. Plug in power cord 2. Replace fuse 3. Replace lamp 4. Remove modules (except power supply) one by one. If lamp lights when a particular module is removed, trouble is in that module. Troubleshoot module. If lamp still does not light, trouble is in power supply. Troubleshoot power supply
No output at SCTE connector of pattern generator	1. No output in VFO mode only indicates defective VFO oscillator 2. No output in crystal mode only indicates defective crystal oscillator or phase-lock circuit 3. No output in any range below .1-.01 msec and no output in the crystal mode indicate defective counter #1.	1. Troubleshoot VFO oscillator board NO347 of pattern generator 2. Troubleshoot crystal oscillator and phase-lock board NO348 of pattern generator 3. Troubleshoot counter #1 board NO347 of pattern generator

Table 5-3

SYSTEM TROUBLESHOOTING CHART (Cont)

Symptom	Probable Cause	Remedy
	4. No output in any range below 1-.1 msec and normal output in the crystal mode indicate defective counter #2	4. Troubleshoot counter #2 board NO348 of pattern generator
	5. No output in any range below 10-1 msec and normal output in crystal mode indicate defective counter #3	5. Troubleshoot counter #3 board NO346 of pattern generator
	6. No output in any mode of operation indicates defective output counters #4, 5, and 6	6. Troubleshoot counters #4 5, and 6 on board NO346 of pattern generator
No output at SD connector of pattern generator	1. Defective pseudorandom shift register generator circuits	1. Troubleshoot shift register board NO345 of pattern generator
	2. Defective CLOCK input from main clock counter #5	2. Troubleshoot counter #5 on board NO346 of pattern generator
When using SCTE clock, crossover point of data at pattern generator SD connector does not occur during negative-to-zero transition of clock signal at SCTE connector	1. Defective clock driver	1. Troubleshoot clock driver on board NO345 of pattern generator
	2. Defective wiring from clock output board. Defective clock output board	2. Troubleshoot pattern generator wiring. Troubleshoot clock output board NO346 of pattern generator

Table 5-3

SYSTEM TROUBLESHOOTING CHART (Cont)

Symptom	Probable Cause	Remedy
When using RX TIMING switch in DATA mode, receiver module will not indicate VFO phase-lock on VFO ERROR meter	1. Defective VFO phase-lock circuit	1. Troubleshoot phase-lock circuits on board NO350 of the receiver module
	2. No clock inputs from pattern generator	2. Troubleshoot clock output divider board NO346 of pattern generator
	3. Defective data slicer circuit	3. Troubleshoot defective slicer circuits on NO350 of receiver module
	4. No data inputs from the data set adapter module	4. Troubleshoot receive data circuits on board NO330 of data set adapter
SYNC ALARM lamp will not go off	1. Re-sync circuits defective (Q4 and Q5 on PC board N39079)	1. Troubleshoot re-sync circuits on board N39079 of receiver module
	2. No output from receiver reference pattern generator to error detection circuits	2. Troubleshoot reference pattern generator circuit on board N39079
	3. No external data (RD) from data slicer	3. Troubleshoot data slicer circuit on board NO350 of receiver module
	4. Defective error detection circuits	4. Troubleshoot error detection circuits on board N39079 of receiver module
	5. Defective sample pulse generator circuits	5. Troubleshoot sample pulse circuits on board N39079 of receiver module

Table 5-3

SYSTEM TROUBLESHOOTING CHART (Cont)

Symptom	Probable Cause	Remedy
No error output on receiver BNC and on rear TB1 connector	1. Defective receiver level converter	1. Troubleshoot A13 on board N39079
	2. Defective error detection circuit	2. Troubleshoot error detection circuits on board N39079
	3. Defective sample pulse generator	3. Troubleshoot sample pulse generator circuit on board N39079
	4. Defective anti lockup counter	4. Troubleshoot A14 and A15 on board N39079
All error counter module display readout tubes fail to light	1. Blown module fuse	1. Replace fuse
	2. Defective wiring	2. Inspect high voltage runs to counter display boards
	3. Defective power supply board	3. Troubleshoot high voltage regulator circuit on power supply board
Individual readout tube fails to light	1. Defective anode resistor	1. Replace anode resistor
	2. Defective wiring	2. Correct lead and solder connections for anode lead (see Figure 6-33)
	3. Defective tube	3. Replace tube
Individual readout tube blurred, single character always lighted, or double character displayed	1. Counters have not been reset after turn-on	1. Reset counters
	2. Shorted lead to ground or to another number lead	2. Inspect for metal sliver short on printed circuit runs between decade counters, decoder drivers, and tubes

Table 5-3

SYSTEM TROUBLESHOOTING CHART (Cont)

Symptom	Probable Cause	Remedy
Error counter module counters do not reset	1. No +5-volt power	1. Troubleshoot power supply board wiring of error counter
	2. Defective RUN-STOP-RESET switch	2. Inspect and replace switch
Counters remain at zero or do not count	1. Defective RUN-STOP-RESET switch or broken line	1. Inspect lines and switch
With errors on receiver BNC output, bit error counter does not count errors	1. Receiver level converter is not functioning	1. Check A13 on PC board N39079 of receiver module
	2. Input errors translator is not functioning	2. Check Q407, Q406, and Q408 of PC board 064-155-000-7 of error counter module
	3. Display mode control or counter control is not functioning	3. Troubleshoot counter display control board 064-149-000-7; if isolated to a DIP, replace board
Block counter does not count or counts erratically	1. Input delayed clock translator inverted is not functioning	1. Check for proper outputs at J704-T, Q412, and J703-A; troubleshoot translator board 064-155-000-7, if necessary
	2. Display mode control or counter control is not functioning	2. Troubleshoot counter display control board 064-155-000-7
	3. Thumbwheel wiring is defective	3. Inspect wiring

Table 5-3

SYSTEM TROUBLESHOOTING CHART (Cont)

Symptom	Probable Cause	Remedy
Error counter module fails to issue resync commands, or does so incorrectly	1. Defective AUTO-MANUAL-RESYNC switch	1. Replace AUTO-MANUAL-RESYNC switch
	2. Defective resync command translator	2. Check Q409 on board 064-155-000-7
	3. Defective recognizer board	3. Replace recognizer board 064-153-000-7
Channel outage detector fails to operate	1. Errors translator of error counter module adjusted improperly	1. Follow calibration instructions outlined in paragraph 5.4.5
	2. Integrator reset timer adjusted improperly	2. Follow calibration instructions outlined in paragraph 5.4.5

5.4 ALIGNMENT

The following paragraphs provide instructions for adjusting the Model 600F to optimize equipment performance. Circuits containing adjustments are the VFO, VFO phase-lock, crystal oscillator, error counter module power supply, and error counter module channel outage and translator circuits. It is suggested that all alignment be checked on a semi-annual basis, or whenever repairs are made to the circuits. Test equipment required for alignment are listed in Table 5-2; the only tool required is a small screwdriver.

5.4.1 VFO ALIGNMENT

The following alignment procedure should be performed together with the VFO phase-lock alignment described in the following paragraph in order to obtain optimum performance from the Model 600F. Perform the VFO alignment as follows:

a. Remove pattern generator from cabinet and reconnect by means of extender cable.

b. Set POWER ON switch to ON position.

c. Set TX CLK switch to SCTE position.

d. Set OPR-CAL switch to CAL position. The OPR-CAL switch, S4, is located on chassis plate of pattern generator module.

e. Set RANGE MS switch to .1-.01 position and rotate vernier dial to 10.00.

f. Adjust frequency potentiometer R20 on pattern generator PC board NO347 for clock cycle of 100 microseconds as measured with an oscilloscope at SCTE BNC connector.

g. Rotate vernier dial to 2.00 and adjust ratio potentiometer R35 (PC obard NO347) for clock cycle of 20 microseconds.

h. Repeat steps e, f, and g until both vernier dial readings are correct.

i. Set POWER ON switch to OFF position and OPR-CAL switch to OPR position. Disconnect extender cable and return pattern generator module to Model 600F cabinet. This completes VFO alignment.

5.4.2 VFO PHASE-LOCK ALIGNMENT

a. Remove receiver module from cabinet and reconnect by means of extender cable. Set POWER ON switch to ON position.

b. Set VFO TIME CONSTANT switch to position 2.

c. Set RANGE MS switch to 1-.1 position and rotate vernier dial to 2.00.

d. With no external data or clock input to the receiver, center VFO ERROR meter, M1, indication by adjusting "meter zero" potentiometer R81 on PC board NO350.

e. Set VFO TIME CONSTANT switch to position 4. If VFO ERROR meter drifts from zero, adjust balance potentiometer R66 on PC board NO350 until there is no drift when switching from position 2 to position 4.

f. Set VFO TIME CONSTANT switch to position 2.

g. Adjust frequency potentiometer R76 on PC board NO350 until signal at SCTE BNC connector on pattern generator module is exactly 200 microseconds. The SCTE output cycle of pattern generator should now be exactly the same for either setting of OPR-CAL switch.

h. Set POWER ON switch to OFF position; disconnect extender cable; and return receiver module to Model 600F cabinet. This completes VFO phase-lock alignment.

5.4.3 CRYSTAL OSCILLATOR ADJUSTMENT

The frequency of quartz crystals Y1 and Y2 (used in positions CR1 and CR2, respectively on the RANGE MS switch) is calculated by multiplying the required pattern rate within the range of 300 to 7200 bps by a factor of 80. The Model 600F as supplied, is normally equipped with

quartz crystals for pattern rates of 4800 bps in the CR1 position and 7200 bps in the CR2 position of RANGE MS switch. The corresponding quartz crystal frequency is 384 kHz for 4800 bps (4.8 x 80) and 576 kHz for 7200 bps (7.2 x 80).

Perform the following steps to adjust the crystal oscillator frequency.

a. Remove pattern generator module from cabinet and reconnect by means of extender cable. Set POWER ON switch to ON position.

b. Set RANGE MS switch to CR1 position.

c. Connect electronic frequency counter to collector of transistor Q5 on PC board NO348 (see Figure 6-20) and adjust piston trimmer capacitor CV1 for proper fundamental frequency output of quartz crystal Y1, as displayed on frequency counter (Y1 frequency is 384 kHz for pattern rate of 4800 bps).

d. With frequency counter still connected to Q5 collector, set RANGE MS switch to CR2 position, and adjust piston trimmer capacitor CV2 for proper fundamental frequency output of quartz crystal Y2, as displayed on frequency counter (Y2 frequency is 576 kHz for pattern rate of 7200 bps).

e. Connect frequency counter to SCTE BNC connector on pattern generator module. Frequency counter should display count of 1/80 times Y1 fundamental frequency when RANGE MS switch is in CR1 position, and 1/80 times Y2 fundamental frequency when in CR2 position.

f. Set POWER ON switch to OFF position; remove test connections, and return pattern generator module to Model 600F cabinet. This completes crystal oscillator adjustment.

5.4.4 ERROR COUNTER MODULE POWER SUPPLY

WARNING

The error counter module operates from a 120 vac power source and employs other high voltages. These voltages are always dangerous to life. Use extreme caution when working on this equipment.

Perform adjustment of the error counter module power supply voltages as follows:

a. Remove error counter module from cabinet and reconnect by means of extender cable.

b. Set POWER ON switch to ON position.

c. Connect oscilloscope between pin 3 (common) and pin 1 (+200 volts) on TB703 (see Figure 6-34).

CAUTION

The high voltage regulator is NOT designed to sustain a short circuit condition. Inadvertent grounding of the +200 v supply may cause damage to this power supply

d. Adjust potentiometer R206 on power supply board A8 (see Figure 6-28) until +200 volts is observed on the oscilloscope.

e. Connect oscilloscope between pin 3 (common) and pin 4 (Vcc) on TB703 (see Figure 6-34).

f. Adjust potentiometer R202 on the power supply board A8 (see Figure 6-28) until +5 volts is observed.

g. Set POWER ON switch to OFF position.

5.4.5 CHANNEL OUTAGE AND TRANSLATOR BOARDS

Perform alignment of the channel outage and translator boards while the error counter module is still connected by means of extender cable.

Proceed as follows:

5.4.5.1 Initial Setup. Perform the initial setup as follows:

a. On data set adapter, connect SD BNC to RD BNC and SCTE BNC to SCR BNC.

b. Set INTERFACE switch to E position and MODE switch to PR position.

c. Set pattern generator TX CLK switch to SCTE position.

d. Set RANGE MS switch to .1-.01 position, and rotate vernier dial to 10.0. This adjust SCTE bit rate to 10 kbs.

e. Set receiver RX TIMING switch to CLOCK position and AUTO-MAN-RESYNC switch to AUTO position.

f. Set error counter RUN-STOP-RESET switch to RUN position.

g. Set POWER ON switch to ON position.

5.4.5.2 Alignment Procedure. Perform alignment of channel outage and translator boards as follows:

a. Set oscilloscope trigger and sweep controls on negative slope, normal trigger, and time base of 2 seconds per graticule division.

b. Attach oscilloscope probe to cathode side of diode CR506 on channel outage indicator board (see Figure 6-31), and adjust potentiometer R525 on board to approximately 3/4 of its travel in the clockwise direction.

c. Observe +5 to negative going pulses on oscilloscope trace, and adjust potentiometer R525 until time duration between

pulses is 10 seconds (5 graticule divisions) ±1/2 second.

d. Move oscilloscope probe to bottom of resistor R517 (base of transistor Q502).

e. Rotate potentiometer R440 on translator board (see Figure 6-29) to fully clockwise position.

f. Insert 50 percent error rate by setting pattern generator TX CLK switch to SCT position; observe the integrating dc level on the oscilloscope trace.

NOTE

The outage alarm circuit disabling level is about 4.9 vdc. The outage alarm will be enabled if the integrator voltage peak does not reach 4.9 volts before it is reset by the 10-second timer.

g. Adjust potentiometer R440 on translator board until the peak of integrator waveform reaches 2.8 volts just before it is reset to zero (see Figure 5-1). This calibrates integrator so that an error rate greater than approximately 25 percent causes channel outage alarm to turn on at end of ten seconds.

h. Set POWER ON switch to OFF position, and return error counter module to the chassis. This completes alignment of the channel outage and translator boards.

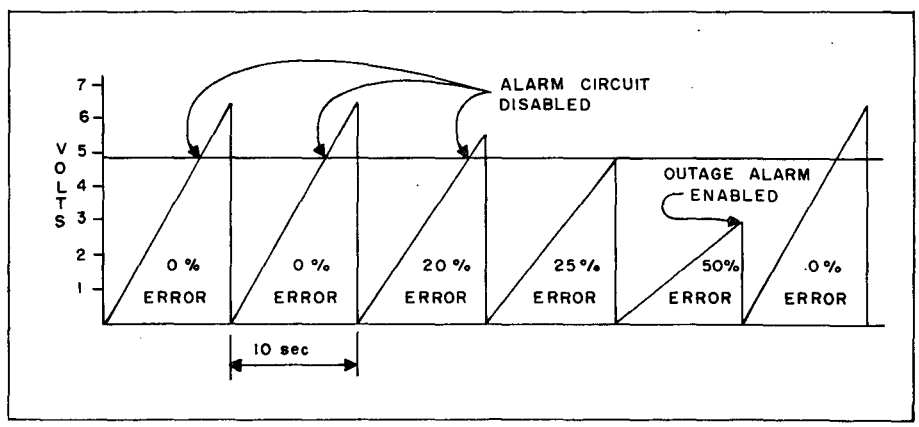


Figure 5-1. Waveform at Base of Q502, Outage Indicator Board

5.4.6 OVERALL PERFORMANCE BENCH TEST

The following test procedures check overall performance of the Model 600F. Proceed as follows:

5.4.6.1 Initial Setup. To perform the initial setup, proceed as follows:

a. Using a "T" connector on SCTE BNC connector, connect a cable between SCTE BNC connector and SCR BNC connector on data set adapter.

b. Using a "T" connector on SD BNC connector, connect a cable between SD BNC connector and RD BNC connector on data set adapter.

c. Connect cable from SCTE BNC "T" connector to channel "A" input of dual trace oscilloscope.

d. Connect cable from SD BNC "T" connector to channel "B" input of oscilloscope.

e. Set pattern generator INSERT ERROR-OFF-SINGLE switch to OFF position and TX CLK switch to SCTE position.

f. Set pattern generator RANGE MS switch to .1-.01 position, and rotate vernier dial to 1.00 position. This adjusts SCTE bit rate to 100 kbs.

g. Set receiver AUTO-MAN-RESYNC switch to AUTO position, VFO TIME CONSTANT switch to 1 position, and RX TIMING switch to DATA position.

h. Set error counter RUN-STOP-RESET switch to STOP position, BLOCK LENGTH thumbwheels to 0001, ERR/BLOCK thumbwheel to 0, and check that the AUTO-CONT switch on the counter display control board is set to AUTO position.

i. Set data set adapter MODE switch to PR position and INTERFACE switch to E position.

j. Set POWER ON switch to ON position.

B

5.4.6.2 Pattern Generator Test Procedure. Perform the following test to check the operation of the shift register and clock generator in the pattern generator module.

a. Observe waveforms on dual trace oscilloscope as follows: channel A—18-volt peak-to-peak squarewave (SCTE) with cycle period of approximately 0.01 millisecond, channel B—18-volt peak-to-peak pseudorandom pattern (SD) with bit length of approximately 0.01 millisecond. Note that pseudorandom pattern is in phase with squarewave.

b. Rotate vernier dial to 10.00 position and observe waveforms on dual trace oscilloscope. Channel A should display 18-volt peak-to-peak squarewave with cycle period of approximately 0.1 millisecond, and Channel B an 18-volt pseudorandom pattern with bit length of approximately 0.1 millisecond.

c. Rotate vernier dial to 1.00 position, and set RANGE MS switch to 1-.1 position. Waveforms observed on oscilloscope should be as in step b.

d. Set RANGE MS switch to 10-1 position. Squarewave and pseudorandom pattern observed on oscilloscope should be same as in step b except that both cycle period and bit length are approximately 1.0 millisecond.

e. Set RANGE MS switch to 100-10 position. Waveforms observed on oscilloscope should be same as in step b except that both squarewave cycle period and pattern bit length are approximately 10 milliseconds.

f. Set RANGE MS switch to CR2 position and then to CR1 position. Waveforms observed on oscilloscope for either position should be same as in step b except that both squarewave cycle period and pattern bit length in milliseconds should be equal to 80 divided by quartz crystal Y2 frequency in kHz for position CR2 and Y1 frequency in kHz for position CR1.

g. Remove oscilloscope connection from SD and SCTE BNC "T" connectors on data set adapter. This completes test

of shift register and clock generator in pattern generator module.

5.4.6.3 VFO Phase-Lock Test Procedure. The VFO phase-lock test procedure checks operation of the VFO phase-lock circuits in the receiver module. Proceed as follows:

a. Connect output of squarewave generator to SCT BNC connector on data set adapter front panel.

b. Set squarewave generator bit rate to 10 bps, and output level to ±6 volts.

c. Connect frequency counter to SCTE BNC connector on data set adapter.

d. On pattern generator module, set RANGE MS switch to 100-10 position. Make fine adjustment on vernier dial to obtain reading of 10.0 Hz on frequency counter.

e. On receiver module, set VFO TIME CONSTANT switch to position 4 and RX TIMING switch to DATA position.

f. Operate AUTO-MANUAL-RESYNC switch momentarily to RESYNC and back to AUTO position. Observe that SYNC ALARM indicator lamp stays lighted.

g. Rock vernier dial on pattern generator very slowly in both directions until SYNC ALARM lamp is extinguished.

h. Set RUN-STOP-RESET switch on error counter to RUN position and note that BLOCKS counter is running and that no bit or block errors are being counted. Also note slight deflection of VFO ERROR meter from center of scale, indicating presence of VFO phase-lock voltage. If bit and block errors are being counted, make fine adjustment on vernier dial until error count is stopped.

i. Rotate vernier dial very slowly in the counter-clockwise direction until BIT ERRORS and BLOCK ERRORS start counting.

j. Return vernier dial to its original position and momentarily set AUTO-MANUAL-RESYNC switch to RESYNC position and then back to AUTO position. SYNC ALARM indicator should light and, simultaneously, all counters should stop, indicating that resynchronization is in progress in receiver module. SYNC ALARM indicator will extinguish and BLOCKS counter will start counting after a few seconds.

k. Set squarewave generator output bit rate to 1000 bps. Note that bit and block errors are being counted.

l. Set RANGE MS switch on pattern generator to 1-.1 position and VFO TIME CONSTANT switch on receiver to 3 position. Errors will continue to be counted for a few seconds before an automatic resynchronization occurs. If SYNC ALARM stays lighted and counters are stopped, make fine adjustment on vernier dial until SYNC ALARM is extinguished and BLOCKS counter starts counting.

m. Rotate vernier dial slowly in counter-clockwise direction and observe VFO ERROR meter deflecting to left of center while no errors are being counted on error counter module. VFO ERROR meter deflection to left indicates phase-lock voltage when VFO is on low side of incoming signal.

n. Rotate vernier dial slowly in clockwise direction and observe VFO ERROR meter deflecting to right of center while no errors are being counted on the error counter module. VFO ERROR meter deflection to right indicates phase-lock voltage when VFO is on high side of incoming signal.

o. Reset vernier dial to its original position and observe VFO ERROR meter returning to center of scale.

p. Set POWER ON switch to OFF. This completes check of VFO phase-lock circuit.

5.4.6.4 Synchronizer and Error Counter Circuits Test Procedure. The synchronizer and error counter circuit test procedure checks the operation of the synchronizer circuits in the receiver module and the

automatic resynchronization circuits and counter displays in the error counter module. Perform the test as follows:

a. Connect cable from SCTE BNC connector to SCR BNC connector and from SD BNC connector to RD BNC connector on data set adapter front panel.

b. Set pattern generator INSERT ERRORS-OFF-SINGLE switch to OFF position and TX CLK switch to SCTE position.

c. Set pattern generator RANGE MS switch to 100-10 position, and rotate vernier dial to 10.00. This adjusts SCTE bit rate to 10 bps.

d. Set receiver AUTO-MANUAL-RESYNC switch to MANUAL position and RX TIMING switch to CLOCK position.

e. Set error counter BLOCK LENGTH thumbwheels to 0001, ERR./BLK thumbwheel to 0 and RUN-STOP-RESET switch to STOP position.

f. Set data set adapter INTERFACE switch to E position and MODE switch to PR position.

g. Set POWER ON switch to ON position.

h. Set RUN-STOP-RESET switch to RUN position, and note that only BLOCKS counter on error module is running.

i. On pattern generator, momentarily set TX CLK switch to SCT and then back to SCTE position. Observe out-of-sync condition with all counters on error counter module running.

j. Momentarily set AUTO-MANUAL-RESYNC switch to RESYNC and then back to MANUAL position. The following events occur simultaneously: SYNC ALARM indicator lights momentarily to indicate resynchronization is in progress; count of bit and block errors stops; and RESYNC indicator lights. This checks operation of synchronizing circuit in receiver module.

k. Turn off RESYNC lamp by depressing RESET switch on error counter module.

l. Momentarily set RUN-STOP-RESET switch to RESET position, and then set to STOP position.

m. Set AUTO-MANUAL-RESYNC switch to AUTO position and RUN-STOP-RESET switch to RUN position.

n. Repeat step i. Note that automatic resynchronization occurs after 50 (but not more than 100) bit errors are counted on error counter module. This checks operation of automatic resynchronization circuit in error counter module when pattern synchronization is lost.

o. Set data set adapter MODE switch to 0 position and note that all counters are running and that no resynchronization is being initiated.

p. Set data set adapter MODE switch to 1 position. Results should be as in step o.

q. Set RUN-STOP-RESET switch to RESET position and then to STOP position. Depress RESET switch to extinguish RESYNC indicator.

r. On data set adapter, disconnect SD BNC connector from RD BNC connector.

s. Set RUN-STOP-RESET switch to RUN; let counter display run for approximately 5 seconds; and then return switch to STOP position.

t. Observe that bit and block errors displayed on error counter are approximately 50 percent of blocks count.

u. Set POWER ON switch to OFF; remove test connections; and return Model 600F to cabinet rack. This completes checkout of the Model 600F.

5.5 PARTS LIST

Parts (except hardware) contained in the Model 600F are listed in Tables 5-4 through 5-11. Items in each table are listed according to assembly figure number, part designator, part description, manufacturers part number, manufacturer, and quantity. A list of manufacturers is provided in Table 5-12.

Table 5-4

PARTS LIST - GENERAL SUB-ASSEMBLY

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-38		Data Transmission Test Set	DO858	FEC	1
6-39	A1	Fan Assembly	CO674	FEC	1
6-38	A2	Pattern Generator Assembly	DO859	FEC	1
6-38	A3	Receiver Assembly	DO860	FEC	1
6-38	A4	Error Counter Assembly	1225	WRE	1
6-38	A5	Power Supply Assembly	DO862	FEC	1
6-38	A6	600F Adapter Assembly	DO863	FEC	1
6-38	A7	Interconnect Cable Harness Assembly	CO489-51	FEC	1
6-38	A8	Extenter Board	CO487	FEC	2
6-38	A9	Cable Assembly "C"	CO786	FEC	1
6-38	J1-J6	Connector	26-190-24	Amphenol-Borg	6

Table 5-4

PARTS LIST - GENERAL SUB-ASSEMBLY (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-38	TB1	Barrier Terminal Strip	5-140-Y	Cinch-Jones	1
6-38	TB2	Barrier Terminal Strip	6-140-Y	Cinch-Jones	1
6-38	E1	Strain Relief	5P-1	Heyman Mfg.	1
6-38	E2, E3	Stand-off Terminal	756	Winchester Electronics	2
6-38	E4	Power Cable	17237	Belden Mfg.	1
6-38	E5-E9	Solder Lug	1416-4	Smith H. H.	6
6-38	J7	Connector	DB-19604-433	ITT Cannon Elec. Co.	1

Table 5-5

PARTS LIST - A1 FAN ASSEMBLY

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-39	A1B1	Motor	1075-08-3439	Howard Industries	1
6-39	A1B1	Blades, fan	6-218-152	Howard Industries	1
6-39	A1B1	Guard	6-182-042	Howard Industries	1
6-39	A1E1, A1E2	Grommet	2170	Smith H. H.	2
6-39	A1E3, A1E4	Terminal, stand-off	753	Winchester Electronics	2
6-39	A1E5	Solder Lug	1416-8	Smith H. H.	1

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-23	A2A1	Random Bit Generator Assembly	DO864	FEC	1
6-22	A2A2	Dividers Assembly	DO865	FEC	1
6-21	A2A3	VFO and Divider Assembly	DO873	FEC	1
6-20	A2A4	Crystal Oscillator and Divider Assembly	DO907	FEC	1
6-24	A2S1	Switch, toggle, SPDT	MST115D	ALCO Elec.	1
6-24	A2S2	Index and Shaft Assembly	P505	Centralab	1
6-24	A2S2	Switch section, ceramic wafer, 11-position	PS21	Centralab	2
6-24	A2S3	Switch, toggle, SPDT	MST105H	ALCO Elec.	1
6-24	A2S4	Switch, slide	G324	Continental-Wirt	1
6-24	A2J1	Connector, PC board	251-15-30-160	Cinch-Jones	1

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-24	A2J2, J3, J4	Connector, PC board	250-15-30-160	Cinch-Jones	3
6-24	A2J5, J6, J7 J9	Connector, BNC	667-6	Dage Elec. Company	4
6-24	A2R1	Potentiometer, 50,000 ohms	AR50K 1%	Helipot Div. of Beckman Instrument	1
6-24	A2P1	Connector	26-159-24	Amphenol-Borg	1
6-24	A2E1	Lug, solder	1416-4	Smith H. H.	1
6-24	A2E2	Knob, duodial vernier	RB	Helipot Div. of Beckman Instrument	1
6-24	A2E3	Knob	50-3-16	Raytheon Co.	1
6-23	A2A1E1	Printed Circuit Board	NO345	FEC	1

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-23	A2A1R1, 3, 4, R8, 10, 11, 12, R16, 18, 19, R20, 24, 26, R27, 28, 32, R34, 35, 36, R40, 42, 43, R44, 48, 50, R51, 52, 56, R58, 59, 60, R64, 66, 67, R68, 72, 74, R75, 76, 80, R82, 83, 84, R88, 90, 91, R93, 95, 97, R98, 99, 100, R105, 106, R107, 113, R117, 119, R120, 121, R122, 125, R135	Resistor, fixed carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Allen-Bradley	63

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-23	A2A1R5, 9, R13, 17, 21, R25, 29, 33, R37, 41, 45, R49, 53, 57, R61, 65, 69, R73, 77, 81, R85, 89, 92, R96, 114, 118, R126	Resistor, fixed carbon comp., 47,000 ohms, 1/4 w, 10%	RC07GF473K	Allen-Bradley	27
6-23	A2A1R6, 7, R14, 15, 22, R23, 30, 31, R38, 39, 46, R47, 54, 55, R62, 63, 70, R71, 78, 79, R86, 87, 94, R115, 116, R124, 127, R130, 133	Resistor, fixed carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Allen-Bradley	30

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-23	A2A1R101, R104, 132	Resistor, fixed carbon comp., 470 ohms, 1/4 w, 10%	RC07GF471K	Allen-Bradley	3
6-23	A2A1R102	Resistor, fixed carbon comp., 1200 ohms, 1/4 w, 10%	RC07GF122K	Allen-Bradley	1
6-23	A2A1R2, R103, 131	Resistor, fixed carbon comp., 120 ohms,. 1/4 w, 10%	RC07GF121K	Allen-Bradley	3
6-23	A2A1R108, R112, 123	Resistor, fixed carbon comp., 22,000 ohms, 1/4 w, 10%	RC07GF223K	Allen-Bradley	3
6-23	A2A1R109	Resistor, fixed carbon comp. 47 ohms, 1/4 w, 10%	RC07GF470K	Allen-Bradley	1
6-23	A2A1R110, R111	Resistor, fixed carbon comp., 1 Megohm, 1/4 w, 10%	RC07GF105K	Allen-Bradley	2
6-23	A2A1R129, R134	Resistor, fixed carbon comp., 10,000 ohms, 1/4 w, 10%	RC07GF103K	Allen-Bradley	2
6-23	A2A1C1-22, C28	Capacitor, fixed ceramic, 220 pf, 500 v	831Z5F221K	Erie Res. Co.	23

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-23	A2A1C23, C26	Capacitor, fixed ceramic, 0.01 μf, 25 v	5835Y5U103Z	Erie Res. Co.	2
6-23	A2A1C24, 25	Capacitor, fixed ceramic, 50 pf, 600 v	831U2M500K	Erie Res. Co.	2
6-23	A2A1C27	Capacitor, fixed ceramic, 820 pf, 500 v	831Z5F821K	Erie Res. Co.	1
6-23	A2A1CR1-35	Diode	1N4009	Gen. Elec.	35
6-23	A2A1Q1-27, Q29, 31-36	Transistor, NPN Silicon	2N3605	Gen. Elec.	34
6-23	A2A1Q28, 30	Transistor, PNP Germanium	2N964	T.I.	2
6-22	A2A2E1	Printed Circuit Board	NO346	FEC	1
6-22	A2A2R1, 2, 6, R8, 9, 10, 14, R16, 17, 18, R22, 24, 25, R26, 30, 32	Resistor, fixed carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Allen-Bradley	16

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-22	A2A2R32, 33, R35-41, 44, R51, 53, 54, R58, 60, 62, R63, 64, 68, R70, 71, 78, R79, 80	Resistor, fixed carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Allen-Bradley	23
6-22	A2A2R3, 7, 11, R15, 19, 23, R27, 31, 34, R46, 50, 55, R59, 65, 69, R72, 77	Resistor, fixed carbon comp., 47,000 ohms, 1/4 w, 10%	RC07GF473K	Allen-Bradley	17
6-22	A2A2R4, 5, 12, R13, 20, 21, R28, 29, 47, R48, 57, 73	Resistor, fixed carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Allen-Bradley	12
6-22	A2A2R42, 56, R66, 67	Resistor, fixed carbon comp., 1500 ohms, 1/4 w, 10%	RC07GF152K	Allen-Bradley	4

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-22	A2A2R43	Resistor, fixed carbon comp., 820 ohms, 1/4 w, 10%	RC07GF821K	Allen-Bradley	1
6-22	A2A2R45, 49	Resistor, fixed carbon comp., 1800 ohms, 1/4 w, 10%	RC07GF182K	Allen-Bradley	2
6-22	A2A2R52, 74 R76	Resistor, fixed carbon comp., 220 ohms, 1/4 w, 10%	RC07GF221K	Allen-Bradley	3
6-22	A2A2R75	Resistor, fixed carbon comp., 470 ohms, 1/4 w, 10%	RC07GF471K	Allen-Bradley	1
6-22	A2A2R61	Resistor, fixed carbon comp., 22,000 ohms, 1/4 w, 10%	RC07GF223K	Allen-Bradley	1
6-22	A2A2C1-8	Capacitor, fixed ceramic, 0.01 μf, 25 v	5835Y5U103Z	Erie Res. Co.	8
6-22	A2A2C9-15	Capacitor, fixed ceramic, 220 pf, 500 v	813Z5F221K	Erie Res. Co.	7
6-22	A2A2CR1-18	Diode	1N270	General Instrument	18

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-22	A2A2Q1-8, Q15, 18, 20, Q23	Transistor, PNP	2N404	Gen. Elec.	12
6-22	A2A2Q9-14, Q19, 21	Transistor, PNP	2N964	T.I.	8
6-22	A2A2Q16, 17, Q22	Transistor, NPN	2N3605	Gen. Elec.	3
6-21	A2A3E1	Printed Circuit Board	NO347	FEC	1
6-21	A2A3R1, 2, 3, R4, 6, 8, 19, R32, 33, 38, R39, 43, 45, R46, 47, 51, R53, 55, 56, R60, 62, 63, R64, 70, 71, R73, 74, 75, R76	Resistor, fixed carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Allen-Bradley	29

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-21	A2A3R5, 31 R34, 40, 44, R48, 52, 57, R61, 65, 69, R72, 77	Resistor, fixed carbon comp., 47,000 ohms, 1/4 w, 10%	RC07GF473K	Allen-Bradley	13
6-21	A2A3R7	Resistor, fixed carbon comp., 12,000 ohms, 1/4 w, 10%	RC07GF123K	Allen-Bradley	1
6-21	A2A3R9, 10, R17	Resistor, fixed carbon comp., 3300 ohms, 1/4 w, 10%	RC07GF332K	Allen-Bradley	3
6-21	A2A3R11, 25, R28, 36, 37, R41, 42, 49, R50, 58, 59, R66, 67	Resistor, fixed carbon comp., 820 ohms, 1/4 w, 10%	RC07GF821K	Allen-Bradley	13
6-21	A2A3R12, 13, R16, 18, 68	Resistor, fixed carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Allen-Bradley	5
6-21	A2A3R14, 15, R24, 30, 78	Resistor, fixed carbon comp., 1200 ohms, 1/4 w, 10%	RC07GF122K	Allen-Bradley	5

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-21	A2A3R20, 35	Potentiometer, WW, 10,000 ohms, 1/2 w	3067P-1-103	Bourns Lab.	2
6-21	A2A3R21, 26	Resistor, fixed carbon comp., 6800 ohms, 1/4 w, 10%	RC07GF682K	Allen-Bradley	2
6-21	A2A3R22, 23	Resistor, fixed carbon comp., 270 ohms, 1/4 w, 10%	RC07GF271K	Allen-Bradley	2
6-21	A2A3R27, 29	Resistor, fixed carbon comp., 3900 ohms, 1/4 w, 10%	RC07GF392K	Allen-Bradley	2
6-21	A2A3R54	Resistor, fixed carbon comp., 470 ohms, 1/4 w, 10%	RC07GF471K	Allen-Bradley	1
6-21	A2A3RT1	Thermistor, disc type, 300 ohms at 25° C	KB23J1	Fenwal	1
6-21	A2A3C1	Capacitor, fixed mica, 620 pf, 500 v, 5%	DM-19-621J	Electro-Motive	1
6-21	A2A3C2	Capacitor, fixed ceramic, 100 pf, 500 v	831Z5F101K	Erie Res. Co.	1

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-21	A2A3C3, 4, 7, C8, 11, 12, 15, C16	Capacitor, fixed ceramic, 220 pf, 500 v	831Z5F221K	Erie Res. Co.	8
6-21	A2A3C5, 6, 9, C10, 13, 14, C17, 18	Capacitor, fixed ceramic, 820 pf, 500 v	831Z5F821K	Erie Res. Co.	8
6-21	A2A3CR1, 19	Diode	1N4009	Gen. Elec.	2
6-21	A2A3CR2, 3	Diode, Zener, 6.8 v	1N4736A	Motorola	2
6-21	A2A3CR4-18	Diode	1N270	General Instrument	15
6-21	A2A3Q1, 2, 6, Q7, 9, 10, 11, Q20	Transistor, PNP Germanium	2N964	T.I.	8
6-21	A2A3Q3, 4, 5, Q8	Transistor, NPN	2N3605	Gen. Elec.	4
6-21	A2A3Q12-19	Transistor, PNP	2N404	Gen. Elec.	8

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-20	A2A4E1	Printed Circuit Board	NC348	FEC	1
6-20	A2A4R1, 4, 8, R11, 17, 19, R20, 21, 25, R27, 29, 33, R37, 39-43, R47, 50, 51, R53, 54, 56, R60, 62, 63, R67, 69, 71, R72, 74, 75, R77, 80, 81, R84-89, 93, R95-97, 101, R103-106, R110, 112, R113, 114, R118, 120, R121, 123-R125	Resistor, fixed carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Allen-Bradley	61

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-20	A2A4R2, 5, R9, 12	Resistor, fixed carbon comp., 1800 ohms, 1/4 w, 10%	RC07GF182K	Allen-Bradley	4
6-20	A2A4R3, 10	Resistor, fixed carbon comp., 33,000 ohms, 1/4 w, 10%	RC07GF333K	Allen-Bradley	2
6-20	A2A4R6, 13	Resistor, fixed carbon comp., 470 ohms, 1/4 w, 10%	RC07GF471K	Allen-Bradley	2
6-20	A2A4R7, 14	Resistor, fixed carbon comp., 1200 ohms, 1/4 w, 10%	RC07GF122K	Allen-Bradley	2
6-20	A2A4R15, 18, R22, 26, 28, R32, 34, 38, R44, 48, 55, R57, 61, 64, R68, 70, 73, R76, 83, 90, R94, 98, 102, R107, 111, R115, 119, R122	Resistor, fixed carbon comp., 47,000 ohms, 1/4 w, 10%	RC07GF473K	Allen-Bradley	28

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-20	A2A4R16, 23, R24, 35, 36, R45, 46, 52, R58, 59, 65, R66, 78, 82, R91, 92, 99, R100, 108, R109, 116, R117	Resistor, fixed carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Allen-Bradley	22
6-20	A2A4R30, 31	Resistor, fixed carbon comp., 820 ohms, 1/4 w, 10%	RC07GF821K	Allen-Bradley	2
6-20	A2A4R49, 79	Resistor, fixed carbon comp., 15,000 ohms, 1/4 w, 10%	RC07GF153K	Allen-Bradley	2
6-20	A2A4C1, 3	Capacitor, fixed ceramic, 0.002 μf, 600 v	801Z5V202P	Erie Res. Co.	2
6-20	A2A4C2, 4	Capacitor, fixed foil film, 0.1 μf, 200 v	192P10492	Sprague Elec.	2

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-20	A2A4C5-14, C16, 17, 20, C21, 24, 25, C28, 29	Capacitor, fixed ceramic, 220 pf, 500 v	831Z5F221K	Erie Res. Co.	18
6-20	A2A4C15, 18, C19, 22, 23, C26, 27, 30	Capacitor, fixed ceramic, 820 pf, 500 v	831Z5F821K	Erie Res. Co.	8
6-20	A2A4CV1, 2	Capacitor, variable, tubular piston trimmer	PC43G520	JFD	2
6-20	A2A4CR1-10	Diode	1N4009	Gen. Elec.	10
6-20	A2A4CR11-CR20	Diode	1N270	General Instrument	10
6-20	A2A4Q1, Q3	Transistor, NPN	2N2857	RCA	2
6-20	A2A4Q2, Q4-23	Transistor, NPN	2N3605	Gen. Elec.	21

Table 5-6

PARTS LIST - A2 PATTERN GENERATOR (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-20	A2A4Q24	Transistor, PNP	2N964	Texas Instr.	1
6-20	A2A4Q25-32	Transistor, PNP	2N404	Gen. Elec.	8
6-20	A2A4Y1	Crystal, quartz	384KHz	McCoy Elec.	1
6-20	A2A4Y2	Crystal, quartz	576KHz	McCoy Elec.	1
6-20	A2A4X1, 2	Socket, crystal	8000-AG3	Augat Inc.	2

Table 5-7

PARTS LIST - A3 RECEIVER MODULE

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-26	A3A1	Assembly, Pattern Synchronizing and Error Detection Circuits	97-0008	Welex Electr.	1
6-25	A3A2	Assembly, Input and Phase-Lock	DO900	FEC	1
6-27	A3S1	Index and Shaft Assembly	P505	Centralab	1
6-27	A3S1	Switch, wafer, ceramic section, 2P-4 position	PA115	Centralab	1
6-27	A3S2	Switch, toggle, 2PDT	MST215N	ALCO Electr.	1
6-27	A3S3	Switch, toggle, SPDT	MST105H	ALCO Electr.	1
6-27	A3DS1	Lamp, incandescent, 28 v, 0.04 amp	327	Gen. Elec.	1
6-27	A3XDS1	Lamp Assembly	162-8430-931	Dialight Corp.	1
6-27	A3M1	Meter, miniature panel type	120	Triplett Elec.	1
6-27	A3J1	Connector	251-15-30-160	Cinch-Jones	1

Table 5-7

PARTS LIST - A3 RECEIVER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-27	A3J2, 3	Connector	250-15-30-160	Cinch-Jones	2
6-27	A3J4, 5, 6	Connector, BNC	667-6	Dage Elec. Co.	3
6-27	A3P1	Connector, 24-pin male	26-159-24	Amphenol-Borg	1
6-27	A3E1	Lug, solder	1416-4	Smith H. H.	1
6-27	A3E2	Knob	50-3-1G	Raytheon Co.	1
6-26	A3A1E1	Printed Circuit Board	N39079	Welex Elec.	1
6-26	A3A1R1	Resistor, fixed carbon comp., 33 ohms, 2 w, 5%	RC42GF330J	Mil. Std.	1
6-26	A3A1R2	Resistor, fixed carbon comp., 150 ohms, 1/4 w, 5%	RC07GF151J	Mil. Std.	1
6-26	A3A1R3, 7, R23	Resistor, fixed carbon comp., 10,000 ohms, 1/4 w, 10%	RC07GF103K	Mil. Std.	3

Table 5-7

PARTS LIST - A3 RECEIVER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-26	A3A1R4, 24	Resistor, fixed carbon comp., 39,000 ohms, 1/4 w, 10%	RC07GF393K	Mil. Std.	2
6-26	A3A1R5	Resistor, fixed carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Mil. Std.	1
6-26	A3A1R6, 11, R15, 17, 18	Resistor, fixed carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Mil. Std.	5
6-26	A3A1R8	Resistor, fixed carbon comp., 1 Megohm, 1/4 w, 10%	RC07GF105K	Mil. Std.	1
6-26	A3A1R9	Resistor, fixed carbon comp., 47 ohms, 1/4 w, 10%	RC07GF470K	Mil. Std.	1
6-26	A3A1R10, 12, R13, 19, 20	Resistor, fixed carbon comp., 6800 ohms, 1/4 w, 10%	RC07GF682K	Mil. Std.	5
6-26	A3A1R14, 16, R25	Resistor, fixed carbon comp., 1200 ohms, 1/4 w, 10%	RC07GF122K	Mil. Std.	3
6-26	A3A1R21, 22	Resistor, fixed carbon comp., 7500 ohms, 1/4 w, 5%	RC07GF752J	Mil. Std.	2

Table 5-7

PARTS LIST - A3 RECEIVER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-26	A3A1R26	Resistor, fixed carbon comp., 820 ohms, 1/4 w, 5%	RC07GF821J	Mil. Std.	1
6-26	A3A1C1	Capacitor, fixed electrolytic, 20 μf, 16 v	TE-1157	Sprague Elec.	1
6-26	A3A1C2	Capacitor, fixed tantalum electro., 0.1 μf, 35 v	150D104X-9035A2	Sprague Elec.	1
6-26	A3A1C3,4	Capacitor, fixed tantalum electro., 0.01 μf, 35 v	150D103X-9035A2	Sprague Elec.	2
6-26	A3A1C5,6	Capacitor, fixed ceramic, 390 pf, 1000v	DD-391	Centralab	2
6-26	A3A1C7,9	Capacitor, fixed mica, 390 pf, 500 v, 5%	DM-15-391J	Electro Motive	2
6-26	A3A1C8,10	Capacitor, fixed ceramic, 1000 pf, 500 v	CE-102	Centralab	2
6-26	A3A1D1	Diode, Zener, 5.6 v	1N752A	Motorola	1

Table 5-7

PARTS LIST - A3 RECEIVER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-26	A3A1D2-6	Diode	1N281	Sylvania	5
6-26	A3A1Q1, 2	Transistor, NPN Silicon	2N3903	Motorola	2
6-26	A3A1Q3, 4, 5	Transistor, PNP Silicon	2N3905	Motorola	3
6-26	A3A1Q6	Transistor, NPN Silicon	2N3053	RCA	1
6-26	A3A1A1	Integrated circuit, 8-Bit Shift Register	SN7491AN	Texas Instr.	1
6-26	A3A1A2, 3	Integrated circuit, Dual J-K Master-Slave flip-flop	SN7473N	Texas Instr.	2
6-26	A3A1A4, 5	Integrated circuit, Monostable Multivibrator	SN15851N	Texas Instr.	2
6-26	A3A1A6-11	Integrated circuit, Quad 2-input NAND gate	SP680A	Signetics	6
6-26	A3A1A12	Integrated circuit, Dual 4-input buffer-driver	SP659A	Signetics	1

Table 5-7

PARTS LIST - A3 RECEIVER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-26	A3A1A13	Integrated circuit, Line Driver	MC1488L	Motorola	1
6-26	A3A1A14	Integrated circuit, 4-Bit Binary Counter	SN7493N	Texas Instr.	1
6-25	A3A2E1	Printed Circuit Board	NO350	FEC	1
6-25	A3A2R1, 4, R29, 32, 38, R42, 46, 49, R51, 74	Resistor, fixed carbon comp., 47,000 ohms, 1/4 w, 10%	RC07GF473K	Allen-Bradley	10
6-25	A3A2R2, 3, R14, 17, 30, R31, 35, 37, R41, 43, 44, R45, 47, 48, R50, 55, 72, R83	Resistor, fixed carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Allen-Bradley	18
6-25	A3A2R5, 13, R20, 28, 62	Resistor, fixed carbon comp., 1200 ohms, 1/4 w, 10%	RC07GF122K	Allen-Bradley	5

Table 5-7

PARTS LIST - A3 RECEIVER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-25	A3A2R6, 10, R24, 27	Resistor, fixed carbon comp., 3900 ohms, 1/4 w, 10%	RC07GF392K	Allen-Bradley	4
6-25	A3A2R7, 8, R25, 26, 78, R79, 80, 82	Resistor, fixed carbon comp., 820 ohms, 1/4 w, 10%	RC07GF821K	Allen-Bradley	8
6-25	A3A2R9, 23	Resistor, fixed carbon comp., 6800 ohms, 1/4 w, 10%	RC07GF682K	Allen-Bradley	2
6-25	A3A2R11, 12, R15, 16, 33, R39, 40, 52, R77, 84	Resistor, fixed carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Allen-Bradley	10
6-25	A3A2R18	Resistor, fixed carbon comp., 22,000 ohms, 1/4 w, 10%	RC07GF223K	Allen-Bradley	1
6-25	A3A2R34, 63	Resistor, fixed carbon comp., 12,000 ohms, 1/4 w, 10%	RC07GF123K	Allen-Bradley	2
6-25	A3A2R36	Resistor, fixed carbon comp., 220 ohms, 1/4 w, 10%	RC07GF221K	Allen-Bradley	1

Table 5-7

PARTS LIST - A3 RECEIVER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-25	A3A2R53, 54, R58	Resistor, fixed carbon comp., 330 ohms, 1/4 w, 10%	RC07GF331K	Allen-Bradley	3
6-25	A3A2R56	Resistor, fixed carbon comp., 68 ohms, 1/4 w, 10%	RC07GF680K	Allen-Bradley	1
6-25	A3A2R57, 73	Resistor, fixed carbon comp., 470 ohms, 1/4 w, 10%	RC07GF471K	Allen-Bradley	2
6-25	A3A2R59	Resistor, fixed carbon comp., 3300 ohms, 1/4 w, 10%	RC07GF332K	Allen-Bradley	1
6-25	A3A2R60	Resistor, fixed carbon comp., 33,000 ohms, 1/4 w, 10%	RC07GF333K	Allen-Bradley	1
6-25	A3A261	Resistor, fixed carbon comp., 330,000 ohms, 1/4 w, 10%	RC07GF334K	Allen-Bradley	1
6-25	A3A2R64	Resistor, fixed carbon comp., 120,000 ohms, 1/4 w, 10%	RC07GF124K	Allen-Bradley	1
6-25	A3A2R65	Resistor, fixed carbon comp., 1.2 Megohms, 1/4 w, 10%	RC07GF125K	Allen-Bradley	1

Table 5-7

PARTS LIST - A3 RECEIVER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-25	A3A2R66	Potentiometer, WW, 10,000 ohms, 1/2 w	3067P-1-103	Bourns Inc.	1
6-25	A3A2R67	Resistor, fixed carbon comp., 10 Megohms, 1/4 w, 10%	RC07GF106K	Allen-Bradley	1
6-25	A3A2R68	Resistor, fixed carbon comp., 470,000 ohms, 1/4 w, 10%	RC07GF474K	Allen-Bradley	1
6-25	A3A2R69, 70	Resistor, fixed carbon comp., 150,000 ohms, 1/4 w, 10%	RC07GF154K	Allen-Bradley	2
6-25	A3A2R71	Resistor, fixed carbon comp., 15,000 ohms, 1/4 w, 10%	RC07GF153K	Allen-Bradley	1
6-25	A3A2R75	Resistor, fixed carbon comp., 470 ohms, 1/2 w, 10%	RC20GF471K	Allen-Bradley	1
6-25	A3A2R76, 81	Potentiometer, WW, 1000 ohms, 1/2 w	3067P-1-102	Bourns Inc.	2
6-25	A3A2C1, 2, 9	Capacitor, fixed ceramic, 100 pf, 500 v	831Z5F101K	Erie Res. Co.	3

Table 5-7

PARTS LIST - A3 RECEIVER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-25	A3A2C3, 4, 5	Capacitor, fixed ceramic, 220 pf, 500 v	831Z5F221K	Erie Res. Co.	3
6-25	A3A2C6	Capacitor, fixed ceramic, 0.01 μf, 25 v	5835Y5U103Z	Erie Res. Co.	1
6-25	A3A2C7	Capacitor, fixed paper dielectric, 0.5 μf, 200 v	P8292ZN12	Aerovox Corp.	1
6-25	A3A2C8	Capacitor, fixed, 5.0 μf, 200 v	156P5052	Sprague Elec.	1
6-25	A3A2CR1, CR3-7, 10, 11	Diode	1N270	General Instruments	8
6-25	A3A2CR8	Diode, Silicon	1N4009	Gen. Elec.	1
6-25	A3A2CR9	Diode, Zener, 8.2 v	1N4738A	Motorola	1
6-25	A3A2CR12	Diode, Zener, 12 v	1N4742A	Motorola	1
6-25	A3A2Q1, 2, 4, Q5, 6, 8, 9, 10, Q11, 12, 21	Transistor, PNP	2N964	Texas Instr.	11

Table 5-7

PARTS LIST - A3 RECEIVER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-25	A3A2Q3, 7, Q19, 20, 22	Transistor, NPN	2N3605	Gen. Elec.	5
6-25	A3A2Q13-17	Transistor, NPN	2N3394	Gen. Elec.	5
6-25	A3A2Q18	Transistor, PNP	2N404	Gen. Elec.	1
6-25	A3A2E2	Clip	6019-29-A	Augat Inc.	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-34	A4C701, 703	Capacitor, fixed electrolytic, 1500 μf, 25 wvdc	TL-1219	Sprague Elec.	2
6-34	A4C702	Capacitor, fixed electrolytic, 4 μf, 450 wvdc	BR4-450	Cornell-Dubilier	1
6-34	A4DS701	Indicator light, white	L-6/50 white	Mura Corp.	1
6-34	A4DS702	Indicator light, amber	L-6/50 amber	Mura Corp.	1
6-34	A4DS703	Indicator light, red	L-6/50 red	Mura Corp.	1
6-34	A4DS704	Relay	10A111BB	Price Elec.	1
6-34	A4F701	Fuse, type 3AG, 1.0 amp, 250 v	312001	Littlefuse	1
6-34	A4Q701	Transistor, NPN	2N3055	Motorola	1
6-34	A4S701-705	Switch, rotary thumbwheel	200030	Eeco	1
6-34	A4S706, 708	Switch, toggle, SPDT	MST-105H	ALCO Elec.	2
6-34	A4S707	Switch, toggle, SPDT	MST-105F	ALCO Elec.	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-34	A4T701	Transformer, power	20458	Torotel, Inc.	1
6-34	A4TB701-703	Terminal strip, 6 terminal slots	MEP-6	ALCO Elec.	3
6-34	A4J701-704	Connector, receptacle, 44-contact	225-22221-101	Amphenol Corp.	4
6-34	A4P701	Connector, pin-polarized, 24 male contacts	26-159-24	Amphenol Corp.	1
6-34	A4XF701	Fuse holder	357001	Littlefuse	1
6-30	A4A1	Recognizer PC Board Assembly	064-152-000-4	WRE	1
6-30	A4A1R601, R602	Resistor, fixed carbon comp., 6800 ohms, 1/4 w, 10%	RC07GF682K	Mil. Std.	2
6-30	A4A1C601-C604	Capacitor, fixed ceramic, 0.1 μf, 10 wvdc	UK10-104	Centralab	4
6-30	A4A1IC601, IC607, 611, IC627	Integrated circuit, quad 2-input positive NAND gate	N7400A	Signetics	4

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-30	A4A1IC602, IC603, 606, IC609, 619, IC623	Integrated circuit, dual D-type edge-triggered flip-flop	N7474A	Signetics	6
6-30	A4A1IC604	Integrated circuit, 8-input positive NAND gate	N7430A	Signetics	1
6-30	A4A1IC605, IC612	Integrated circuit, dual 4-input positive NAND gate	N7420A	Signetics	2
6-30	A4A1IC608, IC613-617	Integrated circuit, 4-bit Binary Counter	N7493A	Signetics	6
6-30	A4A1IC610	Integrated circuit, 8-bit Shift Register	N7491A	Signetics	1
6-30	A4A1IC618	Integrated circuit, quad 2-input Exclusive-OR gate	SN7486N	Texas Instr.	1
6-30	A4A1IC620-IC622, 624, IC625	Integrated circuit, Decade Counter	N7490A	Signetics	5

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-30	A4A1IC626, IC629	Integrated circuit, dual J-K Master-Slave flip-flop	N7473A	Signetics	2
6-30	A4A1IC628	Integrated circuit, triple 3-input positive NAND gate	N7410A	Signetics	1
6-31	A4A2	Outage Indicator PC Board Assembly	064-156-000-4	WRE	1
6-31	A4A2R501, R511	Resistor, fixed carbon comp., 10,000 ohms, 1/2 w, 10%	RC20GF103K	Mil. Std.	2
6-31	A4A2R502	Resistor, fixed carbon comp.,3300 ohms, 1/2 w, 10%	RC20GF332K	Mil. Std.	1
6-31	A4A2R503, A506, 509	Resistor, fixed carbon comp.,330 ohms, 1/2 w, 10%	RC20GF331K	Mil. Std.	3
6-31	A4A2R504, R505, 510	Resistor, fixed carbon comp.,6800 ohms, 1/2 w, 10%	RC20GF682K	Mil. Std.	3
6-31	A4A2R507	Resistor, fixed carbon comp., 47 ohms, 1 w, 10%	RC32GF470K	Mil. Std.	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-31	A4A2R508, R513, 527	Resistor, fixed carbon comp., 100,000 ohms, 1/2 w, 10%	RC20GF104K	Mil. Std.	3
6-31	A4A2R512	Resistor, fixed carbon comp., 1000 ohms, 1/2 w, 5%	RC20GF102J	Mil. Std.	1
6-31	A4A2R515	Resistor, fixed carbon comp., 7500 ohms, 1/2 w, 5%	RC20GF752J	Mil. Std.	1
6-31	A4A2R517	Resistor, fixed carbon comp., 24,000 ohms, 1/2 w, 5%	RC20GF243J	Mil. Std.	1
6-31	A4A2R520	Resistor, fixed carbon comp., 200 ohms, 1/2 w, 5%	RC20GF201J	Mil. Std.	1
6-31	A4A2R523, R526	Resistor, fixed carbon comp., 1 Megohm, 1/2 w, 10%	RC20GF105K	Mil. Std.	2
6-31	A4A2R524	Resistor, fixed carbon comp., 100 ohms, 1/2 w, 5%	RC20GF101J	Mil. Std.	1
6-31	A4A2R525	Potentiometer, 2 Megohms, 1/4 w	MTC26L4	Mallory	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-31	A4A2R528	Resistor, fixed carbon comp., 470 ohms, 1/2 w, 10%	RC20GF471K	Mil. Std.	1
6-31	A4A2C501, C503, 507	Capacitor, fixed ceramic, 0.1 μf, 20 wvdc	UK20-104	Centralab	3
6-31	A4A2C502, C506, 509	Capacitor, fixed ceramic, 0.1 μf, 10 wvdc	UK10-104	Centralab	3
6-31	A4A2C504	Capacitor, fixed tantalum, 1.5 μf, 35 wvdc	196D155X-0035EB	Sprague Elec.	1
6-31	A4A2C505	Capacitor, fixed tantalum, 10 μf, 15 wvdc	196D106X-0015EB	Sprague Elec.	1
6-31	A4A2C508	Capacitor, fixed ceramic, 0.0047 μf, 500 vdc	CK62AW472M	Mil. Std.	1
6-31	A4A2CR501-CR503, 506, CR508, 509	Diode	1N4454	Gen. Elec.	6
6-31	A4A2Q501	Transistor, PNP	2N2905A	Motorola	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-31	A4A2Q502, Q505	Transistor, NPN	2N5172	Gen. Elec.	2
6-31	A4A2Q503, Q508	Transistor, field effect, N-channel	2N5457	Motorola	2
6-31	A4A2Q504, Q507	Transistor, PNP	2N5227	Motorola	2
6-31	A4A2Q506	Transistor, unijunction	2N4871	Motorola	1
6-31	A4A2IC501	Integrated circuit, quad 2-input NAND power gate	MC858P	Motorola	1
6-31	A4A21C502	Integrated circuit, dual D-type edge-triggered flip-flop	N7474A	Signetics	1
6-31	A4A2IC503	Integrated circuit, Hex Inverter (without input diodes)	MC840P	Motorola	1
6-32	A4A3	Counter Display Control PC board Assembly	064-148-000-4	WRE	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-32	A4A3R301, R302, 306	Resistor, fixed carbon comp., 6800 ohms, 1/2 w, 10%	RC20GF682K	Mil. Std.	3
6-32	A4A3R303	Resistor, fixed carbon comp., 100 ohms, 1/2 w, 10%	RC20GF101K	Mil. Std.	1
6-32	A4A3R304, R305	Resistor, fixed carbon comp., 2200 ohms, 1/2 w, 10%	RC20GF222K	Mil. Std.	2
6-32	A4A3R307	Resistor, fixed carbon comp., 47 ohms, 1/2 w, 10%	RC20GF470K	Mil. Std.	1
6-32	A4A3C301-C303, 305-C308	Capacitor, fixed ceramic, 0.1 μf, 10 wvdc	UK10-104	Centralab	7
6-32	A4A3C304	Capacitor, fixed ceramic, 470 pf, 500 v	CE471	Centralab	1
6-32	A4A3CR301-CR325	Diode	1N4454	Gen. Elec.	25

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-32	A4A3IC301-IC305	Integrated circuit, Decade Counter	N7490A	Signetics	5
6-32	A4A3IC306, IC309, 311, IC312	Integrated circuit, quad 2-input positive NAND gate	N7400A	Signetics	4
6-32	A4A3IC307	Integrated circuit, triple 3-input positive NAND gate	N7410A	Signetics	1
6-32	A4A3IC308	Integrated circuit, Hex Inverter (without input diode)	MC840P	Motorola	1
6-32	A4A3IC310	Integrated circuit, dual D-type edge-triggered flip-flop	N7474A	Signetics	1
6-32	A4A3S301	Switch, slide	G-126PC	Continental Wirt	1
6-29	A4A4	Translator PC board Assembly	064-154-000-4	WRE	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-29	A4A4R401, R402, 405, R406, 410, R413, 414, R417, 418, R442	Resistor, fixed carbon comp., 470 ohms, 1/2 w, 10%	RC20GF471K	Mil. Std.	10
6-29	A4A4R403, R407, 411, R415, 419	Resistor, fixed carbon comp., 8200 ohms, 1/2 w, 10%	RC20GF822K	Mil. Std.	5
6-29	A4A4R404, R409, 412, R416, 420, R433, 435	Resistor, fixed carbon comp., 2700 ohms, 1/2 w, 10%	RC20GF272K	Mil. Std.	7
6-29	A4A4R408, R424, 425, R441, 443	Resistor, fixed carbon comp., 560 ohms, 1/2 w, 10%	RC20GF561K	Mil. Std.	5
6-29	A4A4R421, R436	Resistor, fixed carbon comp., 10,000 ohms, 1/2 w, 10%	RC20GF103K	Mil. Std.	2

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-29	A4A4R422, R431, 437	Resistor, fixed carbon comp., 4700 ohms, 1/2 w, 10%	RC20GF472K	Mil. Std.	3
6-29	A4A4R423	Resistor, fixed carbon comp., selected value, 5%	Sel. Value	WRE	1
6-29	A4A4R426, R428, 438, R439	Resistor, fixed carbon comp., 1000 ohms, 1/2 w, 10%	RC20GF103K	Mil. Std.	4
6-29	A4A4R427	Resistor, fixed carbon comp., 20,000 ohms, 1/2 w, 5%	RC20GF203J	Mil. Std.	1
6-29	A4A4R429	Resistor, fixed carbon comp., 6800 ohms, 1/2 w, 10%	RC20GF682K	Mil. Std.	1
6-29	A4A4R430, R432, 434	Resistor, fixed carbon comp., 1800 ohms, 1/2 w, 10%	RC20GF182K	Mil. Std.	3
6-29	A4A4R440	Potentiometer, carbon comp., 10,000 ohms, 1/4 w	U-201	CTS Corp.	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-29	A4A4C401, C403-405, C407	Capacitor, fixed ceramic, 470 pf, 500 v	CE471	Centralab	5
6-29	A4A4C402, C406, 408 C412, 414	Capacitor, fixed ceramic, 0.1 μf, 10 wvdc	UK10-104	Centralab	5
6-29	A4A4C409, C410, 416, C417, 419	Capacitor, fixed ceramic, 220 pf, 1000 wvdc	10TS-T27	Sprague Elec.	5
6-29	A4A4C411, C413, 415	Capacitor, fixed ceramic 0.1 μf, 20 wvdc	UK20-104	Centralab	3
6-29	A4A4CR401, CR402, 403	Diode	1N4454	Gen. Elec.	3
6-29	A4A4Q401-Q405	Transistor, PNP	2N5227	Motorola	5
6-29	A4A4Q406	Transistor, field effect, N-channel	2N5457	Motorola	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-29	A4A4Q408-Q413	Transistor, NPN	2N4124	Motorola	6
6-29	A4A4IC401	Integrated circuit, quad 2-input positive NAND gate	N7400A	Signetics	1
6-29	A4A4IC402	Integrated circuit, quad 2-input buffer	MC857P	Motorola	1
6-33	A4A5, A6, A7	Counter Display PC Board Assembly	064-135-000-4	WRE	3
6-33	A4A5R101-R106	Resistor, fixed carbon comp., 36,000 ohms, 1/4 w, 5%	RC07GF363J	Mil. Std.	6
6-33	A4A5R107, R108	Resistor, fixed carbon comp., 100,000 ohms, 1/4 w, 10%	RC07GF104K	Mil. Std.	2
6-33	A4A5C101-C103	Capacitor, fixed ceramic, 0.1 μf, 10 wvdc	UK10-104	Centralab	3
6-33	A4A5CR101	Diode	1N4454	Gen. Elec.	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-33	A4A5IC101-IC106	Integrated circuit, Decade Counter	N7490A	Signetics	6
6-33	A4A5IC107-IC112	Integrated circuit, BCD-to-Decimal Decoder	N7441B	Signetics	6
6-33	A4A5DS101-DS106	Readout Indicator Tube	B4998	Borroughs	6
6-33	A4A5XDS101-XDS106	Socket, Readout Indicator Tube	SK-178	Borroughs	6
6-28	A4A8	Power Supply Board Assembly	064-144-000-4	WRE	1
6-28	A4A8R201	Resistor, fixed carbon comp., 1500 ohms, 1/2 w, 10%	RC20GF152K	Mil. Std.	1
6-28	A4A8R202	Potentiometer, multiturn, 5000 ohms	Model 79P	Beckman	1
6-28	A4A8R203	Resistor, fixed, 549 ohms, 1%	Type CES	IRC	1
6-28	A4A8R204	Resistor, fixed carbon comp., 470 ohms, 1/2 w, 5%	RC20GF471J	Mil. Std.	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-28	A4A8R205	Resistor, fixed metal film, selected value, 1%	Sel. value	WRE	1
6-28	A4A8R206	Potentiometer, carbon comp., 250,000 ohms, 1/4 w	X201	CTS	1
6-28	A4A8R207	Resistor, fixed carbon comp., 10,000 ohms, 1/2 w, 10%	RC20GF103K	Mil. Std.	1
6-28	A4A8R208	Resistor, fixed carbon comp., 1.3 Megohms, 1/2 w, 5%	RC20GF135J	Mil. Std.	1
6-28	A4A8R209	Resistor, fixed carbon comp., 200,000 ohms, 1/2 w, 5%	RC20GF204J	Mil. Std.	1
6-28	A4A8R210	Resistor, fixed carbon comp., 620 ohms, 1/2 w, 5%	RC20GF621J	Mil. Std.	1
6-28	A4A8R211	Resistor, fixed carbon comp., 3000 ohms, 1/2 w, 5%	RC20GF302J	Mil. Std.	1
6-28	A4A8R212	Resistor, fixed carbon comp., 0.2 ohm, 2 w, 5%	RC42GF0R2J	Mil. Std.	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-28	A4A8R213	Resistor, fixed carbon comp., 750,000 ohms, 1/2 w, 5%	RC20GF754J	Mil. Std.	1
6-28	A4A8C201, C202	Capacitor, fixed ceramic, 4700 pf, 500 vdc	CK62AW472M	Mil. Std.	2
6-28	A4A8C203	Capacitor, fixed tantalum electro., 10 μf, 15 wvdc	196D106X-0015EB	Sprague Elec.	1
6-28	A4A8CR201	Diode	A15F	Gen. Elec.	1
6-28	A4A8CR202, CR203	Diode	JAN1N645	Mil. Std.	2
6-28	A4A8CR204	Diode, Zener, 180 v	1N5279	Motorola	1
6-28	A4A8BR201	Diode, bridge rectifier	VH148	Varo, Inc.	1
6-28	A4A8BR202	Diode, bridge rectifier	VE48	Varo, Inc.	1
6-28	A4A8Q201	Transistor, PNP	2N4918	Motorola	1

Table 5-8

PARTS LIST - A4 ERROR COUNTER MODULE (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-28	A4A8Q202, Q210	Transistor, field effect, N-channel	2N5457	Motorola	2
6-28	A4A8Q203-Q205	Transistor, NPN	2N5089	Motorola	2
6-28	A4A8Q206	Transistor, PNP	2N5401	Motorola	1
6-28	A4A8Q207	Transistor, NPN	2N2219A	Motorola	1
6-28	A4A8Q208	Transistor, NPN	MJE340	Motorola	1
6-28	A4A8Q209	Transistor, NPN	2N5172	Gen. Elec.	1

Table 5-9

PARTS LIST - A5 POWER SUPPLY

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-35	A5R1	Resistor, fixed WW, 27 ohms, 10 w	3764	Ohmite	1
6-35	A5R2	Resistor, fixed WW, 270 ohms, 10 w	3788	Ohmite	1
6-35	A5R3	Resistor, fixed carbon comp., 100 ohms, 1/4 w, 10%	RC07GF101K	Allen-Bradley	1
6-35	A5C1, 2, 3	Capacitor, electrolytic, 4500 μf, 20 v	DCM539-2536-01	Sangamo Elec.	3
6-35	A5L1, 2	Inductor, filter choke	TI-896	Transformers Inc.	2
6-35	A5CR1-6	Diode	1N4002	Texas Instr.	6
6-35	A5CR7	Diode	1N483B	Texas Instr.	1
6-35	A5T1	Transformer, power	TI-895	Transformers Inc.	1
6-35	A5F1	Fuse, 3AG Slo-Blo, 1/2 amp	3AG-313.500	Littlefuse	1

Table 5-9

PARTS LIST - A5 POWER SUPPLY (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-35	A5S1	Switch, toggle	MST115D	ALCO Electr.	1
6-35	A5S2	Switch, slide	G326	Continental Wirt	1
6-35	A5DS1	Bulb, incandescent, 28 v, 0.04 amp	327	Gen. Elec.	1
6-35	A5XDS1	Lamp Assembly (green)	162-8430-932	Dialight Corp.	1
6-35	A5XF1	Fuseholder	4405	Bussman Mfg.	1
6-35	A5P1	Connector	26-159-24	Amphenol	1
6-35	A5TB1	Terminal Board	B1021	FEC	1

Table 5-10

PARTS LIST - A6 DATA SET ADAPTER (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-37	A6A1	Assembly, Level Converters	DO867	FEC	2
6-37	A6S2	Switch, toggle, SPDT	MST115D	ALCO Elec.	1
6-37	A6S3	Switch, rotary, 4-pole, 2-position	PS113	Centralab	1
6-37	A6S4	Switch, rotary, 3-pole, 3-position	PS103	Centralab	1
6-37	A6DS1-4	Lamp, incandescent, 14 v, 0.08 amp	330	Gen. Elec.	4
6-37	A6X1-4	Lamp assembly	162-8430-932	Dialight Corp.	4
6-37	A6J1, 2	Connector	251-15-30-160	Cinch-Jones	2
6-37	A6P1, 2	Connector	26-159-24	Amphenol-Borg	2
6-37	A6TP1-5	Connector, BNC	667-6	Dage	5
6-37	A6R1	Resistor, fixed carbon comp., 390 ohms, 1/2 w, 10%	RC20GF391K	Allen-Bradley	1

Table 5-10

PARTS LIST - A6 DATA SET ADAPTER (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-37	A6R2	Resistor, fixed carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Allen-Bradley	1
6-37	A6C1, 2	Capacitor, fixed metalized paper dielectric, 0.033 μf, 200 v	P123ZNP033	Aerovox	2
6-37	A6C3	Capacitor, fixed ceramic dielectric, 0.022 μf, 100 v	855-502X5VO-203Z	Erie Res.	1
6-37	A6L1, 2	Inductor, 50 μh	NR-56	Lenox, Fugle	2
6-37	A6E1	Printed Circuit Board	NO355	FEC	1
6-37	A6E2	Lug, solder	1416-4	Smith H. H.	1
6-37	A6E3, 4	Knob	50-3-1G	Raytheon	2
6-37	A6A1E1	Printed Circuit Board	NO330	FEC	2
6-36	A6A1R1, 19	Resistor, fixed carbon comp., 39,000 ohms, 1/4 w, 10%	RC07GF393K	Allen-Bradley	2
6-36	A6A1R2, 3, R13, 20, 21, R31, 38, 55	Resistor, fixed carbon comp., 12,000 ohms, 1/4 w, 10%	RC07GF123K	Allen-Bradley	8

Table 5-10

PARTS LIST - A6 DATA SET ADAPTER (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-36	A6A1R4, 22, R53	Resistor, fixed carbon comp., 47,000 ohms, 1/4 w, 10%	RC07GF473K	Allen-Bradley	3
6-36	A6A1R5, 23	Resistor, fixed carbon comp., 100 ohms, 1/4 w, 10%	RC07GF101K	Allen-Bradley	2
6-36	A6A1R6, 15, R24, 33, 37, R54	Resistor, fixed carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Allen-Bradley	6
6-36	A6A1R7, 8, R25, 26	Resistor, fixed carbon comp., 1500 ohms, 1/4 w, 10%	RC07GF152K	Allen-Bradley	4
6-36	A6A1R9, 27	Resistor, fixed carbon comp., 2700 ohms, 1/4 w, 10%	RC07GF272K	Allen-Bradley	2
6-36	A6A1R10, 28	Resistor, fixed carbon comp., 3900 ohms, 1/4 w, 10%	RC07GF392K	Allen-Bradley	2
6-36	A6A1R11, 29, R61	Resistor, fixed carbon comp., 470 ohms, 1/4 w, 10%	RC07GF471K	Allen-Bradley	3

Table 5-10

PARTS LIST - A6 DATA SET ADAPTER (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-36	A6A1R12, 30, R58, 64	Resistor, fixed carbon comp., 6800 ohms, 1/4 w, 10%	RC07GF682K	Allen-Bradley	4
6-36	A6A1R14, 32	Resistor, fixed carbon comp., 22,000 ohms, 1/4 w, 10%	RC07GF223K	Allen-Bradley	2
6-36	A6A1R16, 34, R39, 42, 43, R48, 49, 52, R56	Resistor, fixed carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Allen-Bradley	9
6-36	A6A1R17, 35	Resistor, fixed carbon comp., 15,000 ohms, 1/4 w, 10%	RC07GF153K	Mil. Std.	2
6-36	A6A1R18, 36	Resistor, fixed carbon comp., 1000 ohms, 1/4 w, 10%	RC07GF102K	Mil. Std.	2
6-36	A6A1R40, 41, R46, 47, 59	Resistor, fixed carbon comp., 3300 ohms, 1/4 w, 10%	RC07GF332K	Allen-Bradley	5
6-36	A6A1R44, 51	Resistor, fixed carbon comp., 47 ohms, 1/4 w, 10%	RC07GF470K	Allen-Bradley	2

Table 5-10

PARTS LIST - A6 DATA SET ADAPTER (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-36	A6A1R45, 50	Resistor, fixed carbon comp., 470 ohms, 1/2 w, 10%	RC20GF471K	Allen-Bradley	2
6-36	A6A1R56	Resistor, fixed carbon comp., 3000 ohms, 1/4 w, 10%	RC07GF302K	Mil. Std.	1
6-36	A6A1R57	Resistor, fixed carbon comp., 240 ohms, 1/4 w, 10%	RC07GF241K	Allen-Bradley	1
6-36	A6A1R60	Resistor, fixed carbon comp.,	RC07GF331K	Allen-Bradley	1
6-36	A6A1R62, 63	Resistor, fixed carbon comp., 150 ohms, 1 w, 10%	RC32GF151K	Mil. Std.	2
6-36	A6A1C1-4	Capacitor, fixed ceramic, 50 pf, 600 v	831U2M500K	Erie Res. Co.	4
6-36	Q6A1Q1, 4, Q7, 10, 14, Q18-22	Transistor, NPN	2N3394	Gen. Elec.	10

Table 5-10

PARTS LIST - A6 DATA SET ADAPTER (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
6-36	A6A1Q2, 3, Q5, 8, 9, 11, Q16	Transistor, NPN	2N3605	Gen. Elec.	7
6-36	A6A1Q6, 12, Q13	Transistor, PNP	2N964	Texas Instr.	3
6-36	A6A1Q15	Transistor, PNP	40319	RCA	1
6-36	A6A1Q17	Transistor, PNP	2N4037	RCA	1

Table 5-11

PARTS LIST - A7 HARNESS ASS'Y, A8 EXTENDER BOARD & CABLE ASS'Y "C"

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
	A7P1	Connector, P/O harness assembly	26-159-24	Amphenol-Borg	1
	A7J1	Connector, P/O harness assembly	26-190-24	Amphenol-Borg	1
	A8J1	Connector, P/O extender board	251-15-30-160	Cinch-Jones	1
	A8E1	Printed Circuit Board	NO161	FEC	1
	A9P1, 2	Connector, P/O cable assembly "C"	DB19604-432	ITT Cannon	2
	A9E1, 2	Back shell, P/O A9P1 and P2	DB51226-1	ITT Cannon	2

Table 5-12

LIST OF MANUFACTURERS

Manufacturer	Manufacturer's Address
Aerovox	Aerovox Corporation 740 Belleville Avenue New Bedford, Massachusetts 02741
ALCO Elec.	ALCO Electronics Products, Incorporated 3 Walcott Avenue Lawrence, Massachusetts 01843
Allen-Bradley	Allen-Bradley Company 1201 South 2nd Street Milwaukee, Wisconsin 53204
Amphenol-Borg	The Bunker-Ramo Corporation Amphenol Connector Division 2801 South 25th Avenue Broadview, Illinois 60153
Augat	Augat Incorporated 33 Perry Avenue Attleboro, Massachusetts 02703
Belden	Belden Corporation 415 South Kilpatrick Chicago, Illinois 60644
Borroughs	Borroughs Manufacturing Company 3002 North Burdick Kalamazoo, Michigan 49007
Bourns	Bourns Incorporated Trimpot Products Division 1200 Columbia Avenue Riverside, California 92507

Table 5-12

LIST OF MANUFACTURERS (Cont)

Manufacturer	Manufacturer's Address
Bussman	Bussman Manufacturing Division of McGraw-Edison Company 2536 West University Street St. Louis, Missouri 63017
Centralab	Globe Union Incorporated Centralab Division P.O. Box 591 Milwaukee, Wisconsin 53201
Cinch-Jones	Cinch Manufacturing Company and Howard B. Jones Division 1026 South Homan Avenue Chicago, Illinois 60624
Continental-Wirt	Continental-Wirt Electronics Corporation 26 West Queen Street Philadelphia, Pennsylvania 19144
Cornell-Dubilier	Cornell-Dubilier Electronics Division Federal Pacific Electric Company 50 Paris Street Newark, New Jersey 07105
CTS	CTS Corporation 1142 West Beardsley Avenue Elkhart, Indiana 46514
Dage Elec.	The Bendix Corporation Microwave Devices Division Hurricane Road Franklin, Indiana 46131
Dialight Corp.	Dialight Corporation 60 Stewart Avenue Brooklyn, New York 11237

Table 5-12

LIST OF MANUFACTURERS (Cont)

Manufacturer	Manufacturer's Address
Eeco	Engineered Electronics Company Incorporated 1441 East Chestnut Avenue Santa Ana, California 92701
Electro-Motive	The Electro Motive Manufacturing Company Incorporated South Park and John Streets Willimantic, Connecticut 06226
Erie Res.	Erie Technological Products Incorporated 644 West 12th Street Erie, Pennsylvania 16512
Fenwal	Fenwal Electronics, Incorporated 63 Fountain Street Framingham, Massachusetts 01701
FEC	Frederick Electronics Corporation P.O. Box 502 Frederick, Maryland 21701
Gen. Elec.	General Electric Company Semiconductor Products Department Electronics Park Syracuse, New York 13201
General Instruments	General Instruments Corporation Rectifier Division 65 Gouverneur Street Newark, New Jersey 07014
Helipot Div. of Beckman	Beckman Instruments, Incorporated Helipot Division 2500 Harbor Boulevard Fullerton, California 92634

Table 5-12

LIST OF MANUFACTURERS (Cont)

Manufacturer	Manufacturer's Address
Heyman	Heyman Manufacturing Company 147 North Michigan Avenue Kenilworth, New Jersey 07033
Howard Industries	Howard Industries Division of MSL Industries, Incorporated 1760 State Street Racine, Wisconsin 53404
ITT Cannon	ITT Cannon Electric, Incorporated 3208 Humbolt Street Los Angeles, California 90031
JFD	JFD Electronics Corporation 15th at 62nd Street Brooklyn, New York 11219
Lenox-Fugle	Lenox Fugle Electronics, Incorporated 100 Sylvania Place South Plainfield, New Jersey 07080
Littelfuse	Littelfuse, Incorporated 800 East Northwest Highway Des Plaines, Illinois 60016
McCoy Elec.	McCoy Electronics Company Watts-Chestnut Street Mt. Holly Springs, Pennsylvania 17065
Mil. Std.	Military Standard
Motorola	Motorola Semiconductor Products, Incorporated 5005 East McDowell Road Phoenix, Arizona 85008

Table 5-12

LIST OF MANUFACTURERS (Cont)

Manufacturer	Manufacturer's Address
Mura	Mura Corporation 355 Great Neck Road Great Neck, New York 11021
Ohmite	Ohmite Manufacturing Company 3601 West Howard Street Skokie, Illinois 60076
Price Elec.	Price Electric Company Division of North American Phillips Corporation 5560 Church Street Frederick, Maryland 21701
Raytheon	Raytheon Company, Components Division, Industrial Components Operation 465 Centre Quincy, Massachusetts 02169
RCA	RCA Corporation Solid State Division Route 202 Somerville, New Jersey 08876
Sangamo	Sangamo Electric Company South Carolina Division Pickens, South Carolina 29671
Signetics	Signetics Corporation 811 East Argues Avenue Sunnyvale, California 94086
Smith H. H.	Smith Herman H., Incorporated 812 Snediker Avenue Brooklyn, New York 11207

Table 5-12

LIST OF MANUFACTURERS (Cont)

Manufacturer	Manufacturer's Address
Sprague	Sprague Electric Company North Adams, Massachusetts 01247
Sylvania	Sylvania Electronic Products Incorporated Semiconductor Division 100 Sylvan Road Woburn, Massachusetts 01801
Texas Instr.	Texas Instruments, Incorporated Semiconductor Components Division 13500 North Central Expressway Dallas, Texas 75231
Torotel	Torotel, Incorporated 13402 South 71 Highway Grandview, Missouri 64030
Transformers, Inc.	Transformers, Incorporated 4116 Howard Avenue Kensington, Maryland 20795
Triplett	Triplett Corporation 286 Harmon Road Bluffton, Ohio 45817
Varo	Varo, Incorporated Semiconductor Division 1000 North Shiloh Garland, Texas 75040
Welex	Halliburton Company Welex Electronics-Elcor Division Box 986, Silver Spring, Maryland 20910

Table 5-12

LIST OF MANUFACTURERS (Cont)

Manufacturer	Manufacturer's Address
WRE	Western Reserve Electronics, Incorporated 12430 Euclid Avenue Cleveland, Ohio 44106
Winchester Electronics	Winchester Electronics Division Litton Industries, Incorporated Main Street and Hillside Avenue Oakville, Connecticut 06779

G

SECTION 6

DRAWINGS

This section includes all schematic and assembly diagrams of printed circuit boards contained in each module of the Model 600F Data Transmission Test Set, wiring and assembly diagrams of each module, and a rear panel wiring diagram. In addition, an overall functional block diagram of the Model 600F is included to show the relationship of circuits contained in the modules.

Tables 1 and 2 are lists of schematic, wiring and assembly diagrams contained in this section. An overall functional block diagram of the Model 600F is provided in Figure 6-40.

Table 6-1

SCHEMATIC AND WIRING DIAGRAMS

Table 6-1

SCHEMATIC AND WIRING DIAGRAMS (Cont)

Table 6-2

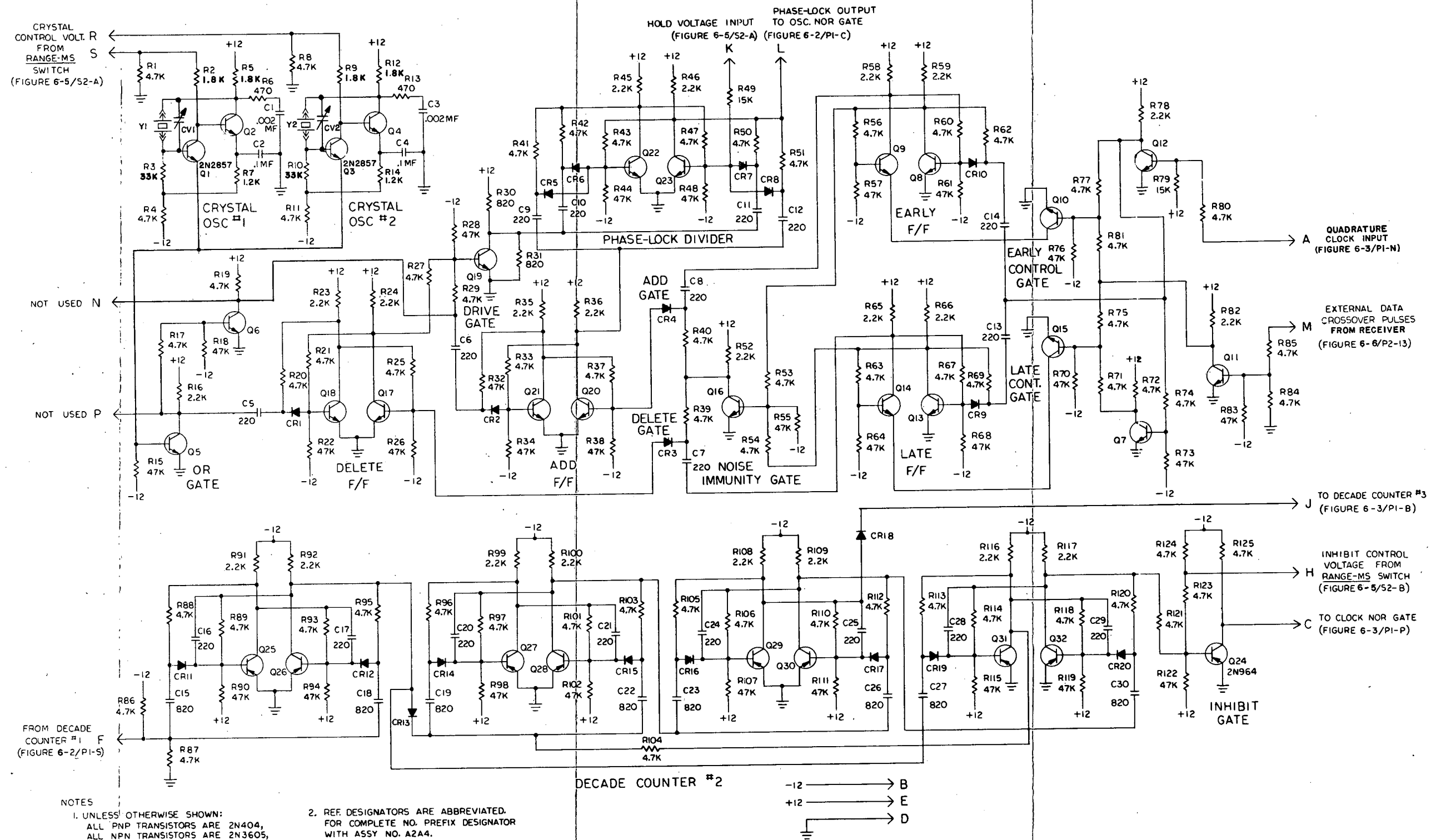
ASSEMBLY DRAWINGS

Table 6-2

ASSEMBLY DRAWINGS (Cont)

FOLDOUT FRAME 1

FOLDOUT FRAME 2



NOTES

1. UNLESS OTHERWISE SHOWN:
   ALL PNP TRANSISTORS ARE 2N404,
   ALL NPN TRANSISTORS ARE 2N3605,
   ALL DIODES ARE 1N4009 EXCEPT
   CR11 THRU CR20 ARE 1N270,
   ALL RESISTORS ARE 1/4 W, ±10%,
   ALL CAPACITOR VALUES ARE PICOFARADS
2. REF. DESIGNATORS ARE ABBREVIATED. FOR COMPLETE NO. PREFIX DESIGNATOR WITH ASSY NO. A2A4.
3. PLUG DESIGNATION P1.
4. P.C. BOARD REF. NO348.
5. BOARD ASSY REF 00907.
6. OSCILLATOR DESIGNED FOR FREQUENCIES FROM 24 KC TO 240 KC. Y1 & Y2 WILL VARY PER CUSTOMER REQUIREMENT.
7. Q1 AND Q3 ARE RCA TYPE 2N2857.

Figure 6-1. Crystal Oscillators and Crystal Phase-Lock Circuits Schematic Diagram

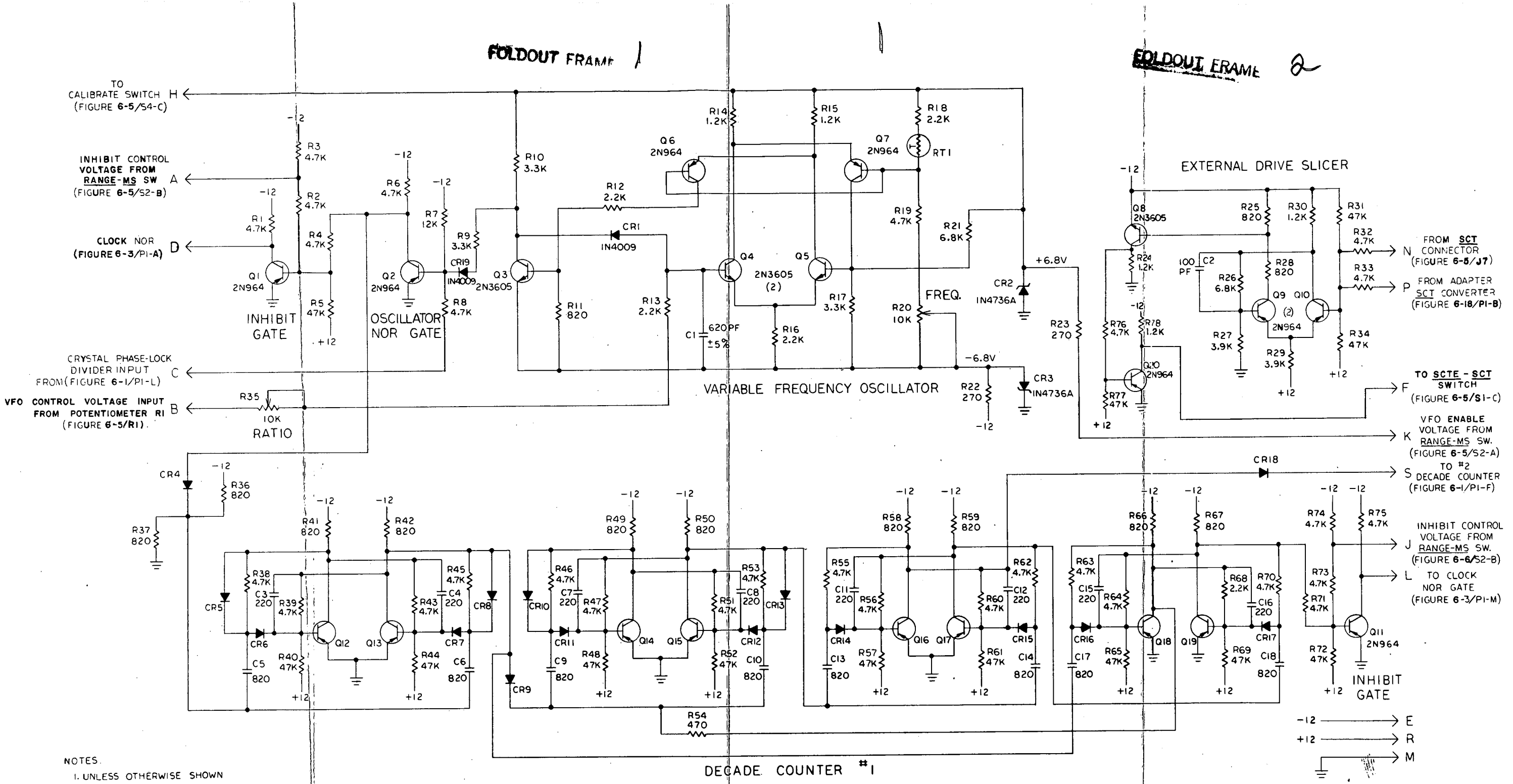
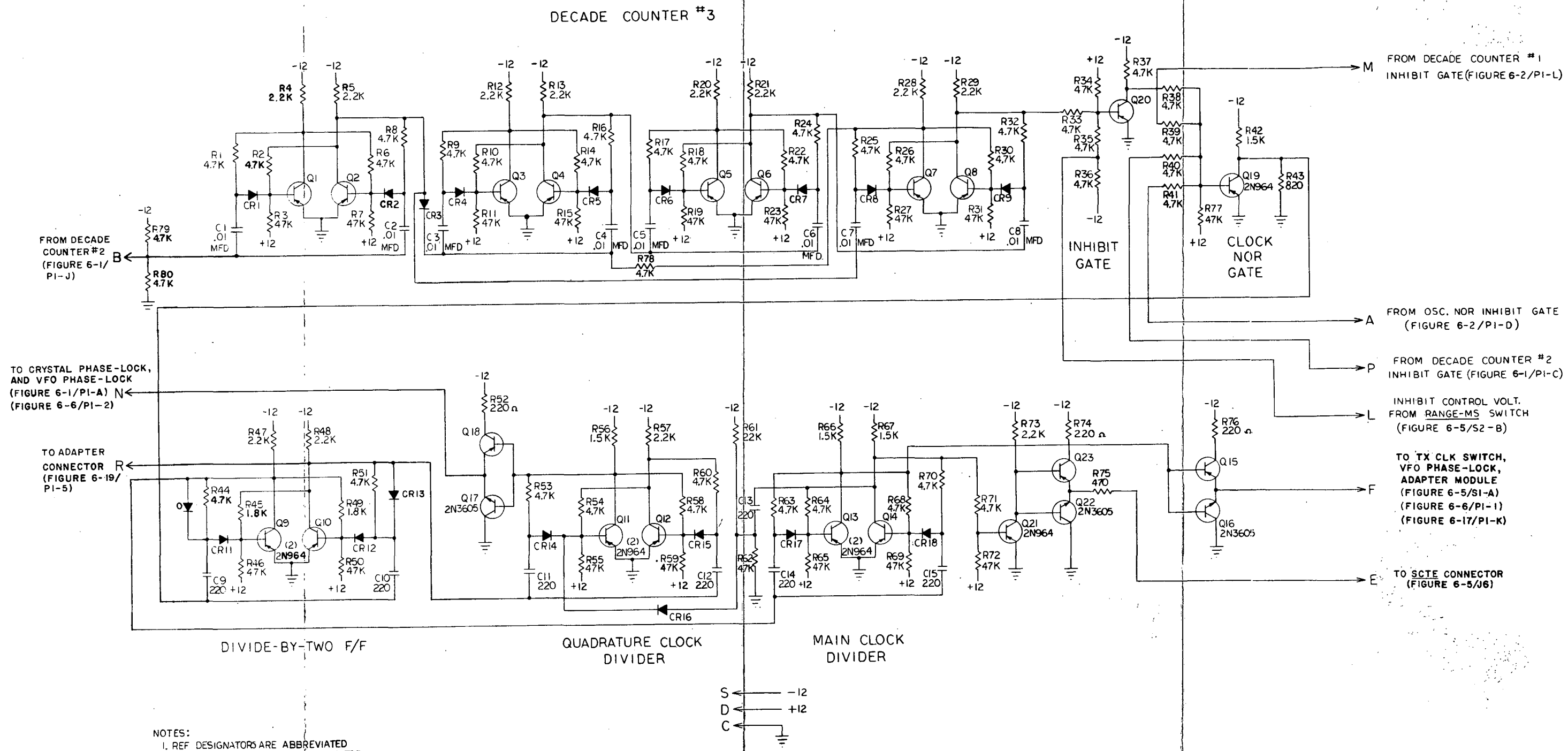


Figure 6-2. Variable Frequency Oscillator and Decade Counter No. 1 Schematic Diagram

FOLDOUT FRAME 1

1

FOLDOUT FRAME 2



NOTES:
1. REF DESIGNATORS ARE ABBREVIATED FOR COMPLETE NO. PREFIX DESIGNATOR WITH ASSY NO. A2A2
2. UNLESS OTHERWISE SPECIFIED, DIODES ARE IN270, TRANSISTORS ARE 2N404, CAPACITORS ARE IN PICOFARADS, RESISTORS ARE 1/4 WATT ±10%.
3. PLUG DESIGNATOR IS P1
4. REF. P.C. BOARD NO346
5. REF. ASSY. D0865

Figure 6-3. Divider Circuits Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

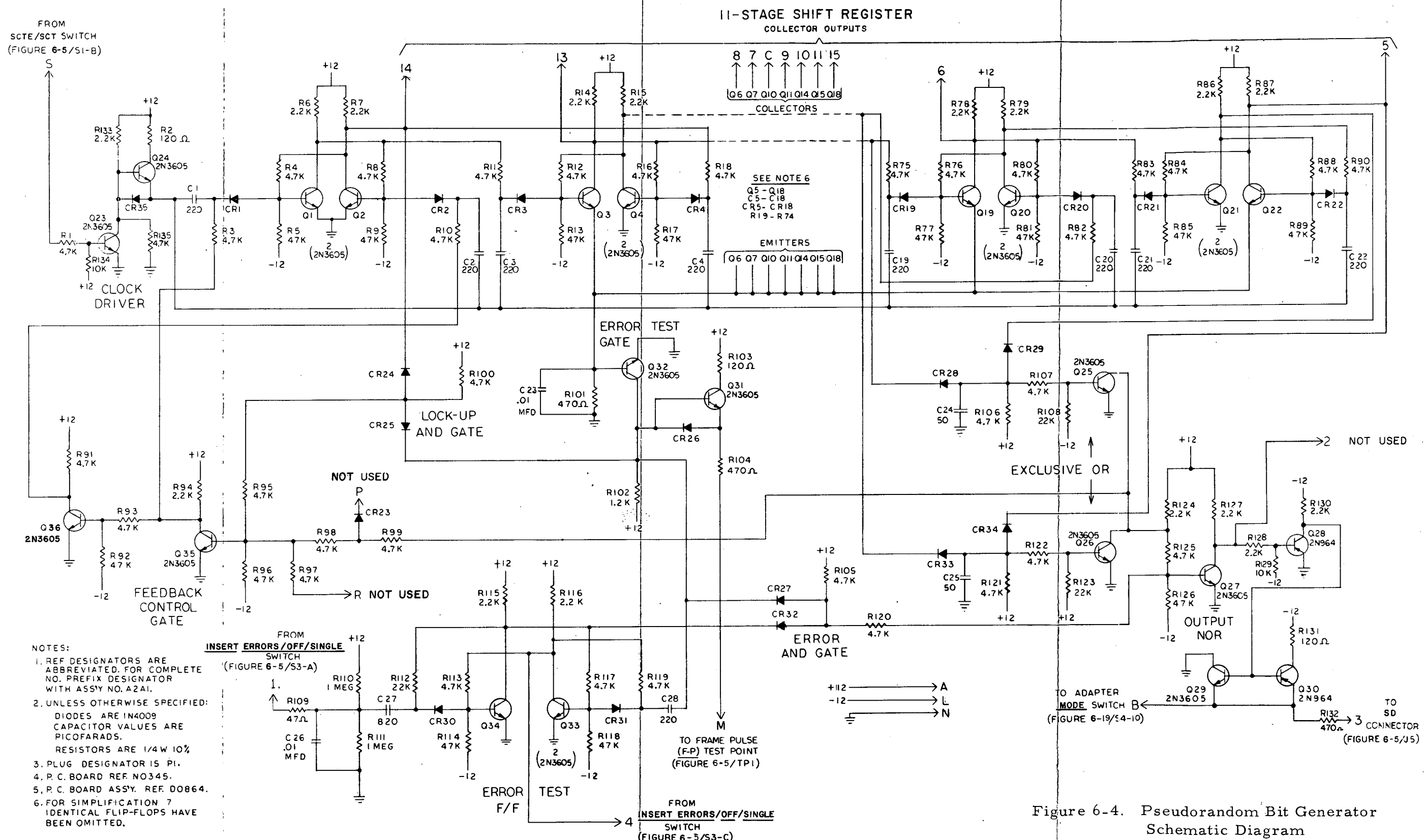
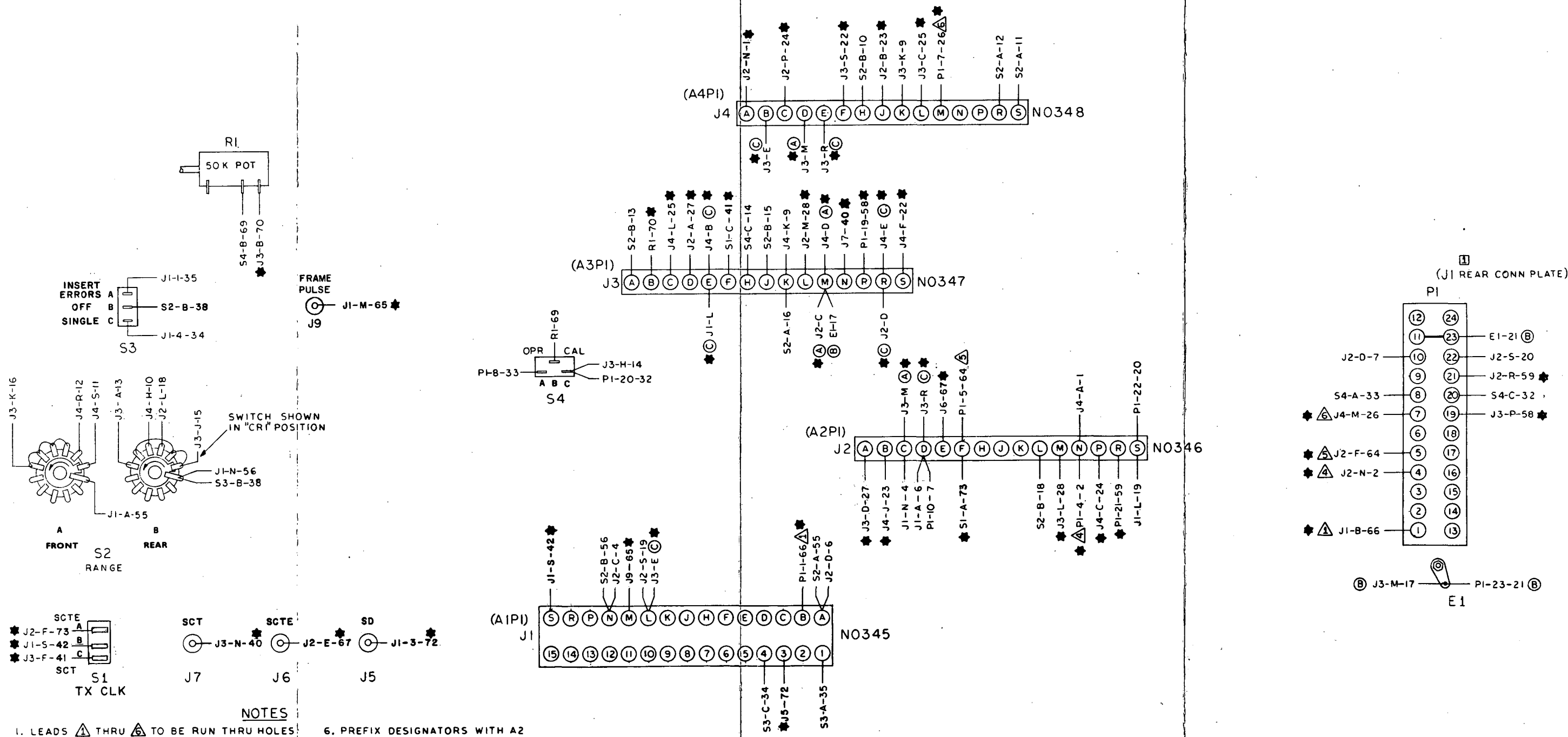


Figure 6-4. Pseudorandom Bit Generator Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2



NOTES

1. LEADS ⚠1 THRU ⚠6 TO BE RUN THRU HOLES IN BRACKETS COUNTING FROM J1 SIDE OF CHASSIS.
2. ✱ THESE LEADS TO RUN DIRECT WITH A MINIMUM OF SLACK.
3. (A) NO.18 BUSS
4. (B) NO.18 WIRE, STRANDED
5. (C) NO.22 BUSS, INSULATED
6. PREFIX DESIGNATORS WITH A2 EXCEPT 1

Figure 6-5. Pattern Generator Wiring Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

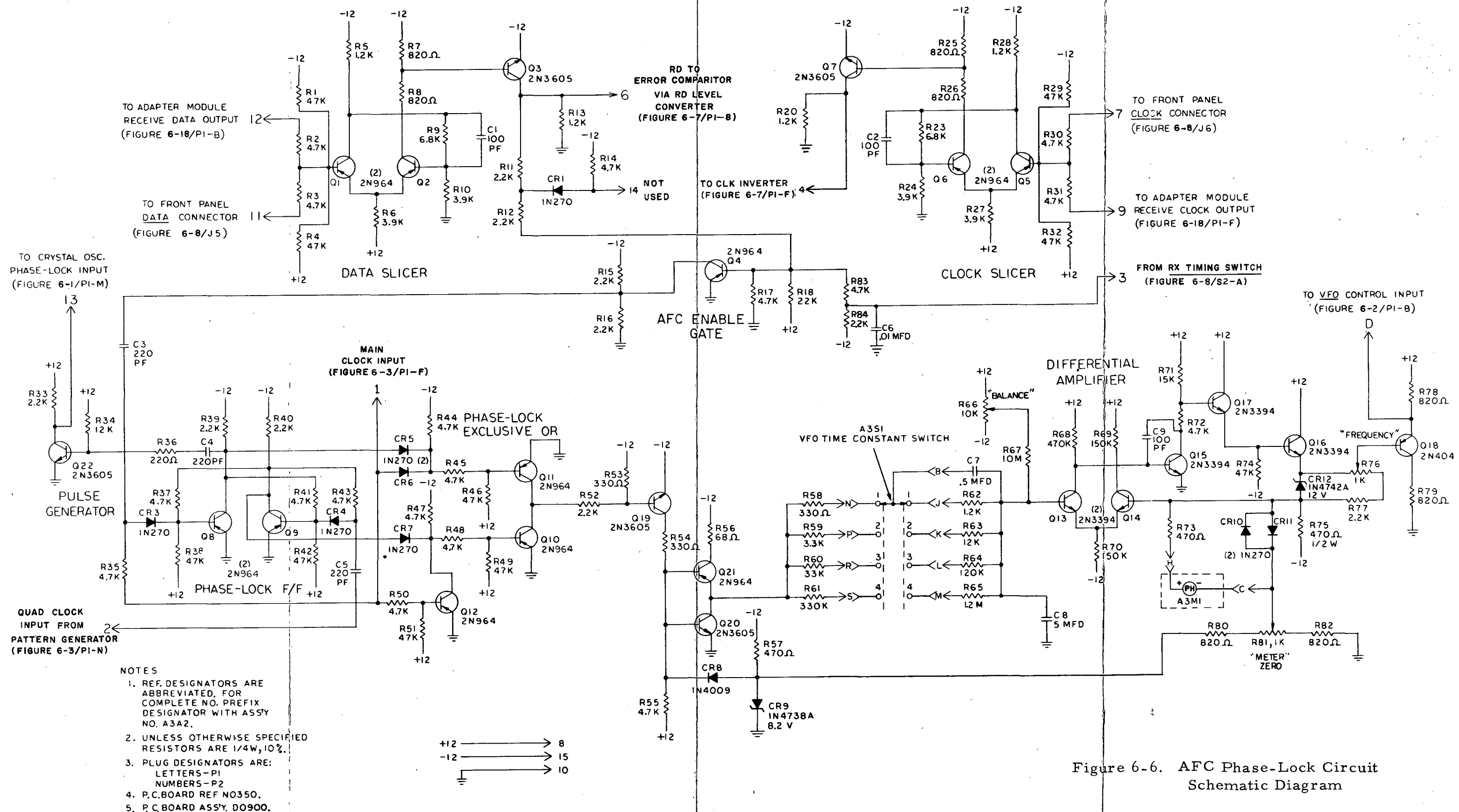


Figure 6-6. AFC Phase-Lock Circuit Schematic Diagram

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FOLDOUT FRAME 1

FOLDOUT FRAME 2

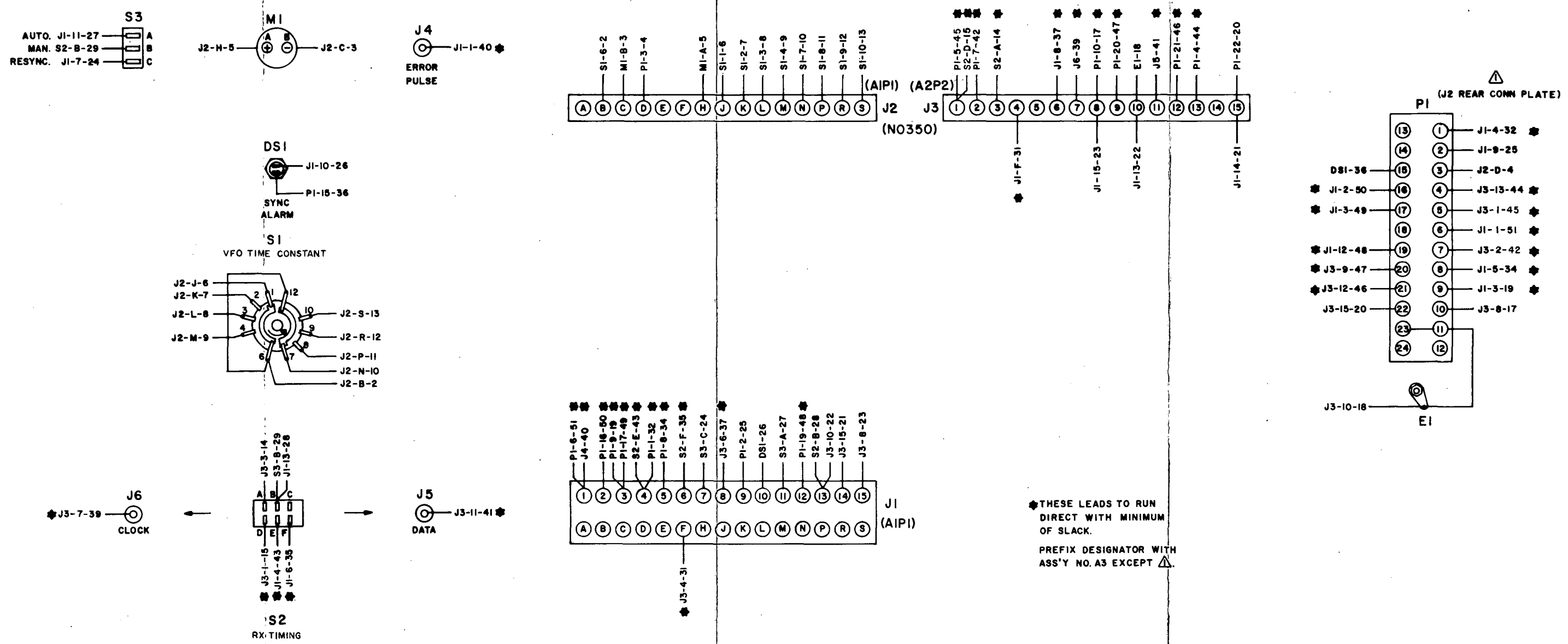

Figure 6-8. Receiver Module Wiring Diagram

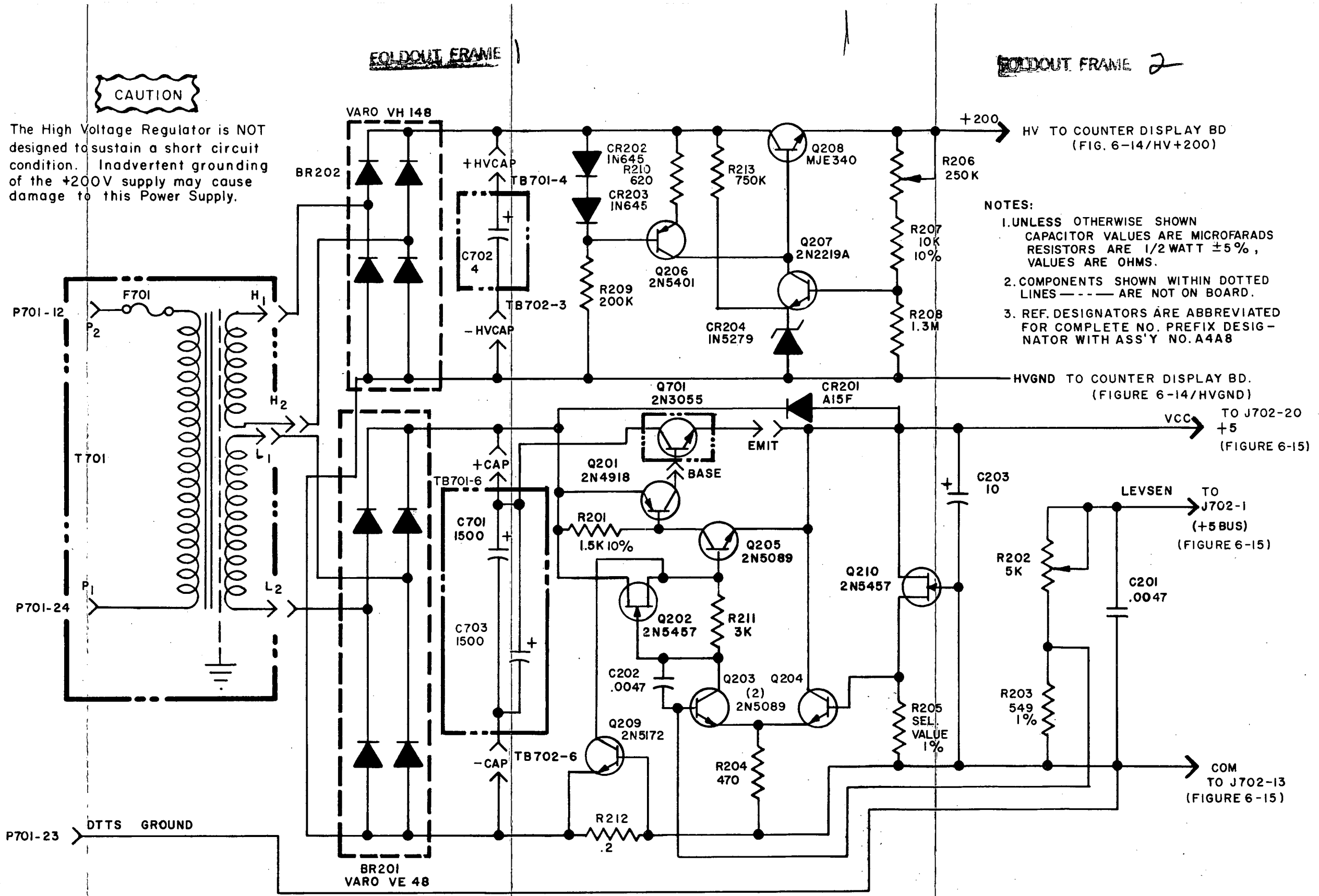

Figure 6-9. Power Supply Board Schematic Diagram

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FOLDOUT FRAME 1

FOLDOUT FRAME 2

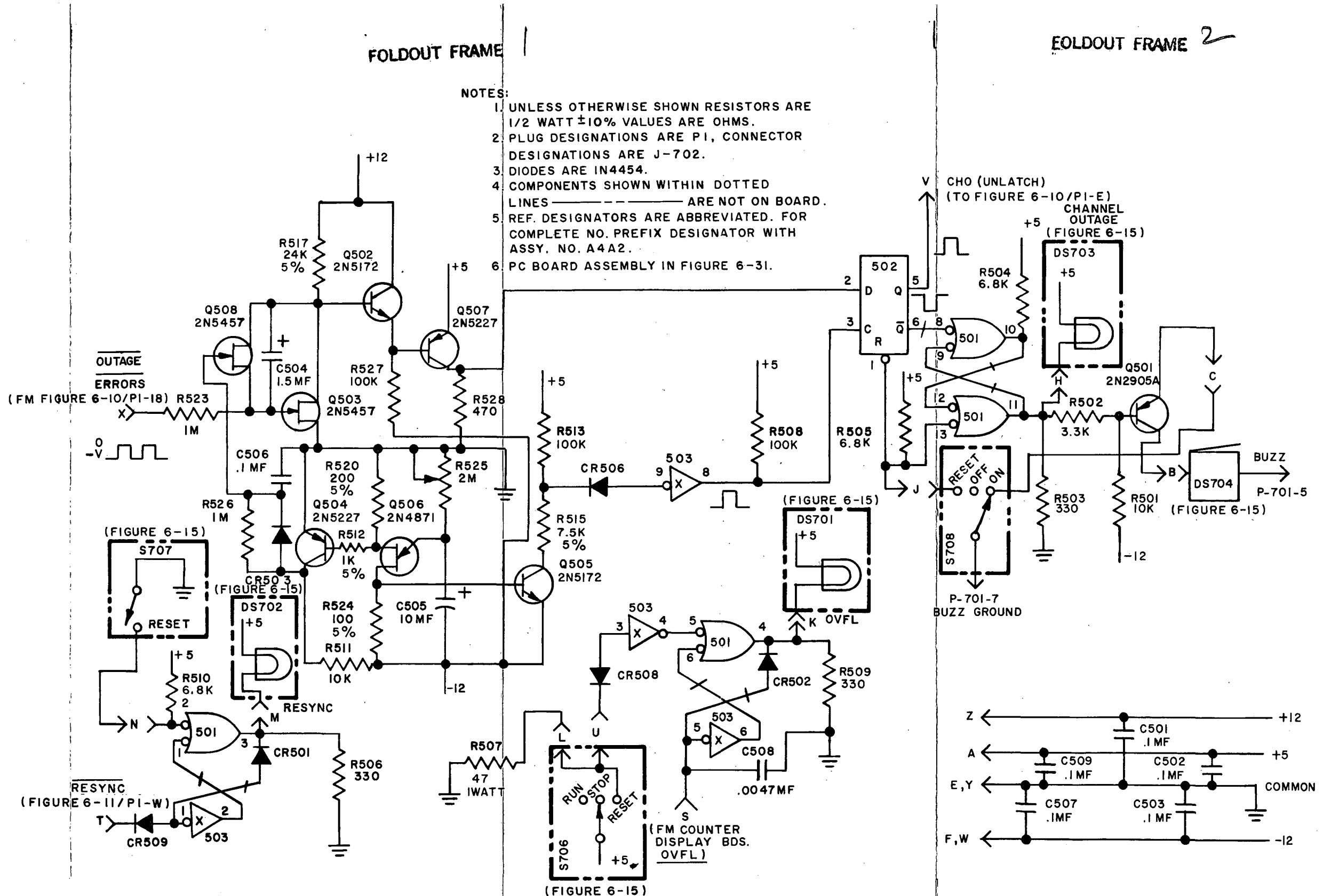

Figure 6-12. Outage Indicator Board Schematic Diagram

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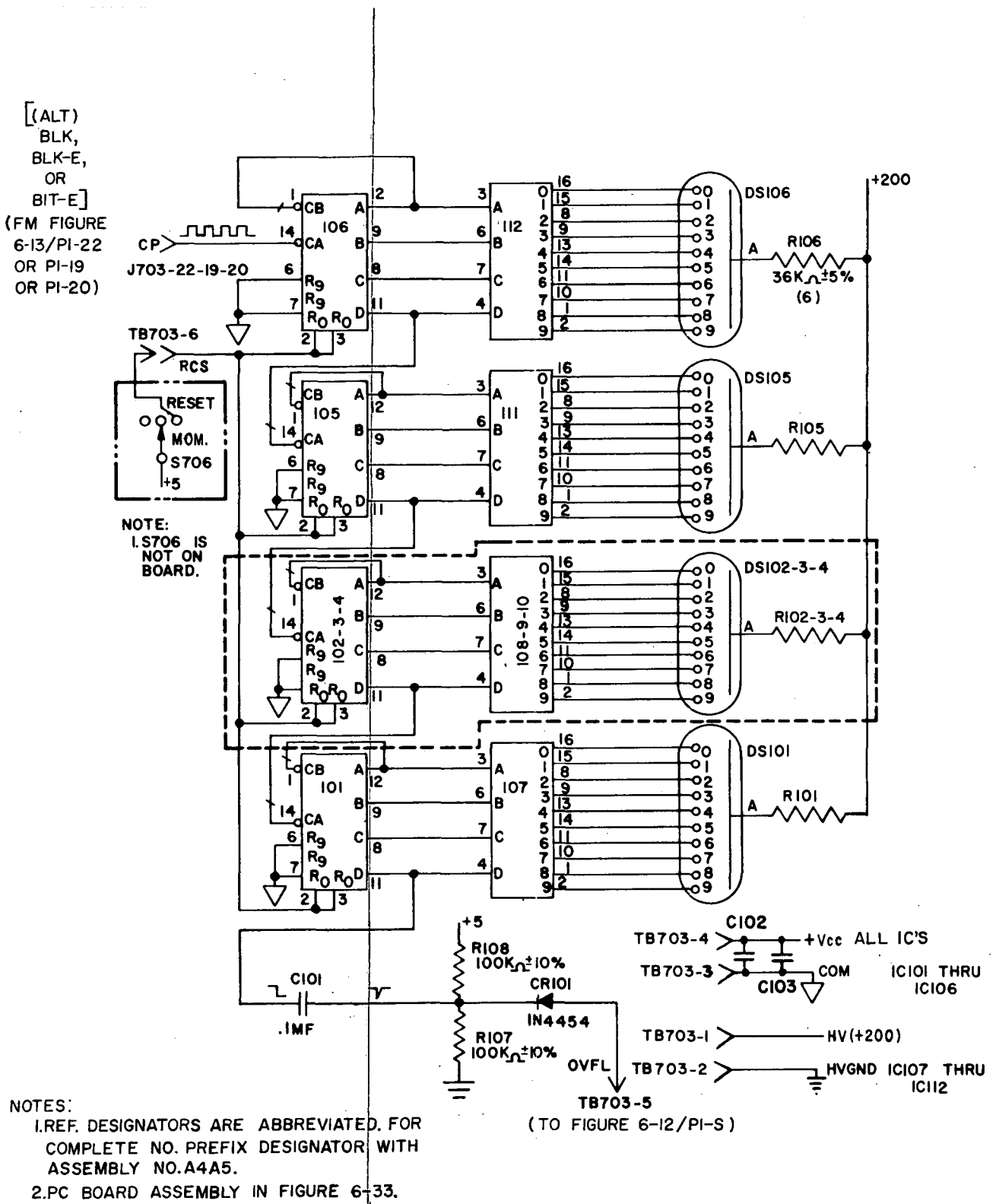

Figure 6-14. Counter Display Board Schematic Diagram

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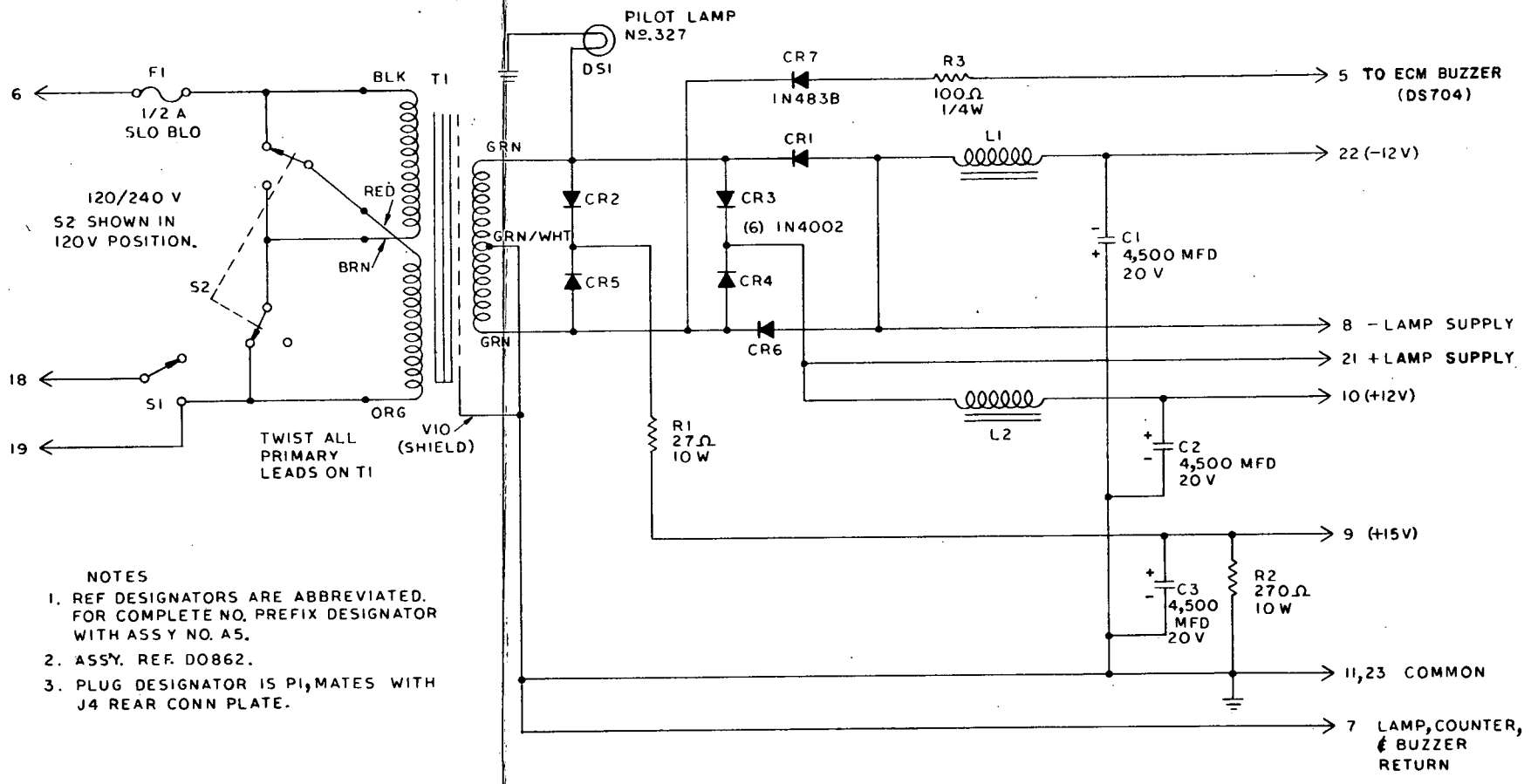


Figure 6-16. Power Supply Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

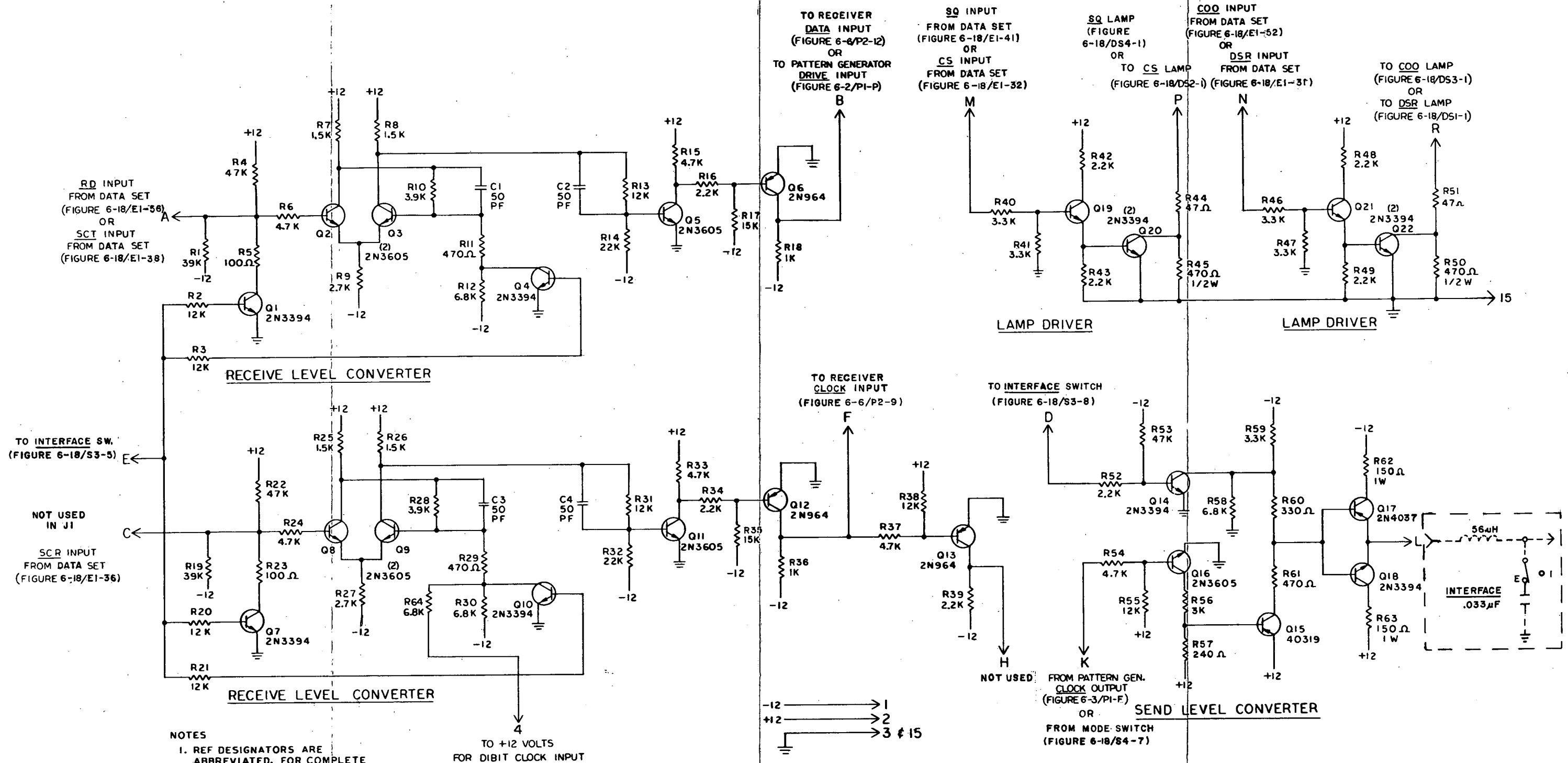
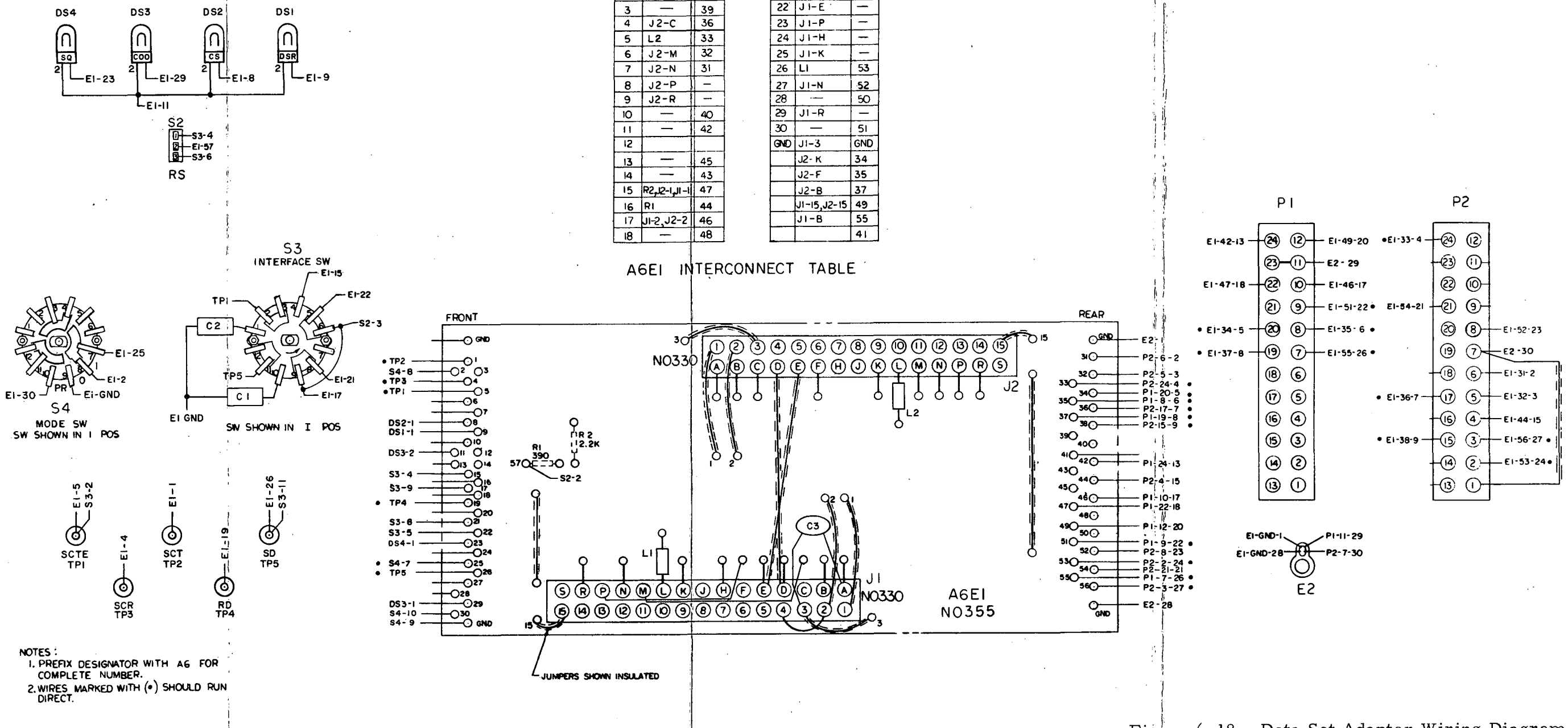


Figure 6-17. Data Set Adapter Schematic Diagram

FOLDOUT FRAME

FOLDOUT FRAME 2



FRONT		REAR
GND	J2-3	GND
1	J2-A	38
2	R2	—
3	—	39
4	J2-C	36
5	L2	33
6	J2-M	32
7	J2-N	31
8	J2-P	—
9	J2-R	—
10	—	40
11	—	42
12		
13	—	45
14	—	43
15	R2,J2-1,J1-1	47
16	R1	44
17	J1-2, J2-2	46
18	—	48

FRONT		REAR
19	J1-A	56
20	J1-M	54
21	J1-D	—
22	J1-E	—
23	J1-P	—
24	J1-H	—
25	J1-K	—
26	L1	53
27	J1-N	52
28	—	50
29	J1-R	—
30	—	51
GND	J1-3	GND
	J2-K	34
	J2-F	35
	J2-B	37
	J1-15, J2-15	49
	J1-B	55
		41

A6EI INTERCONNECT TABLE

NOTES:
1. PREFIX DESIGNATOR WITH A6 FOR COMPLETE NUMBER.
2. WIRES MARKED WITH (•) SHOULD RUN DIRECT.

Figure 6-18. Data Set Adapter Wiring Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

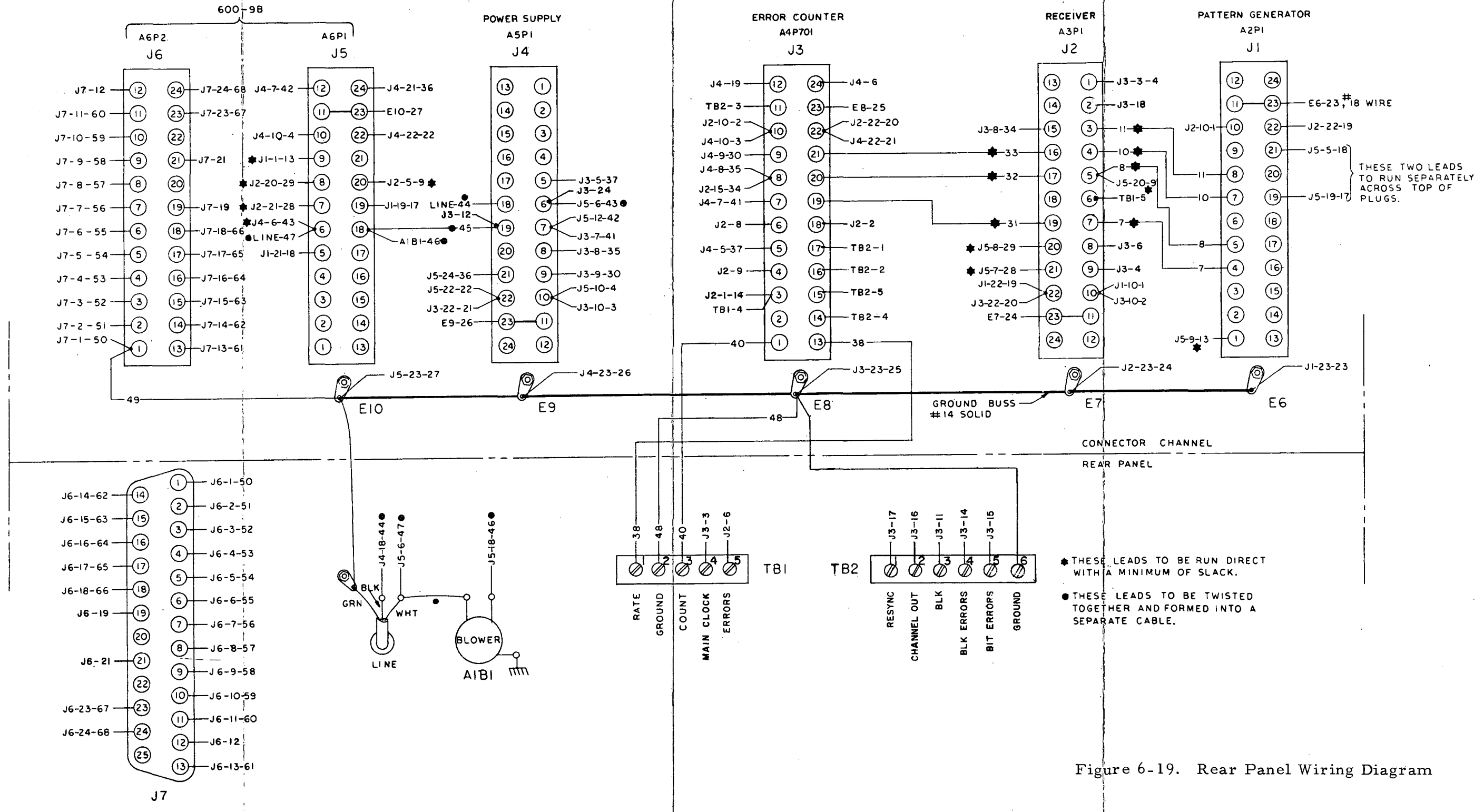


Figure 6-19. Rear Panel Wiring Diagram

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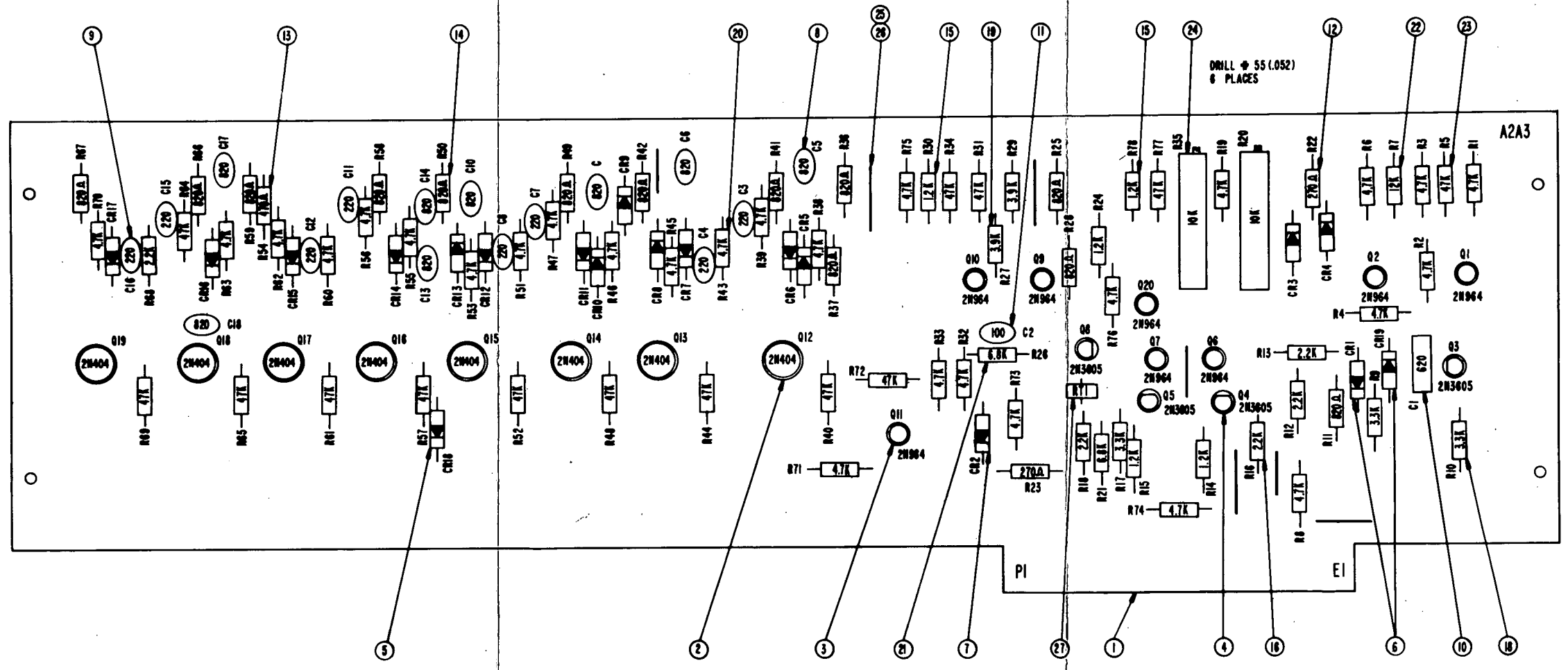
FOLDOUT FRAME 1

FOLDOUT FRAME 2

ITEM	REQD	PART NO	DESCRIPTION	MAN. OR MFR.
27	1	K823J1	THERMISTOR	FENWAL
26	A/R		TUBING, INSUL. 22 AWG.	ALPHA
25	A/R		WIRE, SOLID, 22 AWG.	ALPHA
24	2	3067P-103	TRIM-POT 10K	BOURNS
23	13	RC07GF473K	RESISTOR 47K 1/4 W, ± 10%	A-B
22	1	123	12K	
21	2	682	6.8K	
20	29	472	4.7K	
19	2	392	3.9K	
18	3	332	3.3K	
17				
16	5	222	2.2K	
15	5	122	1.2K	
14	13	821	820 Ω	
13	1	471	470 Ω	
12	2	RC07GF271K	RESISTOR 270 Ω 1/4 W, ± 10%	A-B
11	1	831Z5FD101K	CAPACITOR 100 PF 500 V	ERIE
10	1	DM-19-621J	CAPACITOR 620 PF 500 V	ELEC.MOT.
9	8	831Z5F221K	CAPACITOR 220 PF 500 V	ERIE
8	8	831Z5F821K	CAPACITOR 820 PF 500 V	ERIE
7	2	1N4736A	ZENER DIODE	MOT.
6	2	1N4009	DIODE	G.E.
5	15	1N270	DIODE	G.I.
4	4	2N3605	TRANSISTORS	G.E.
3	8	2N964	TRANSISTORS	T.I.
2	8	2N404	TRANSISTORS	G.E.
1	1	NO347	PC BOARD	FEC

LIST OF MATERIAL



NOTES :

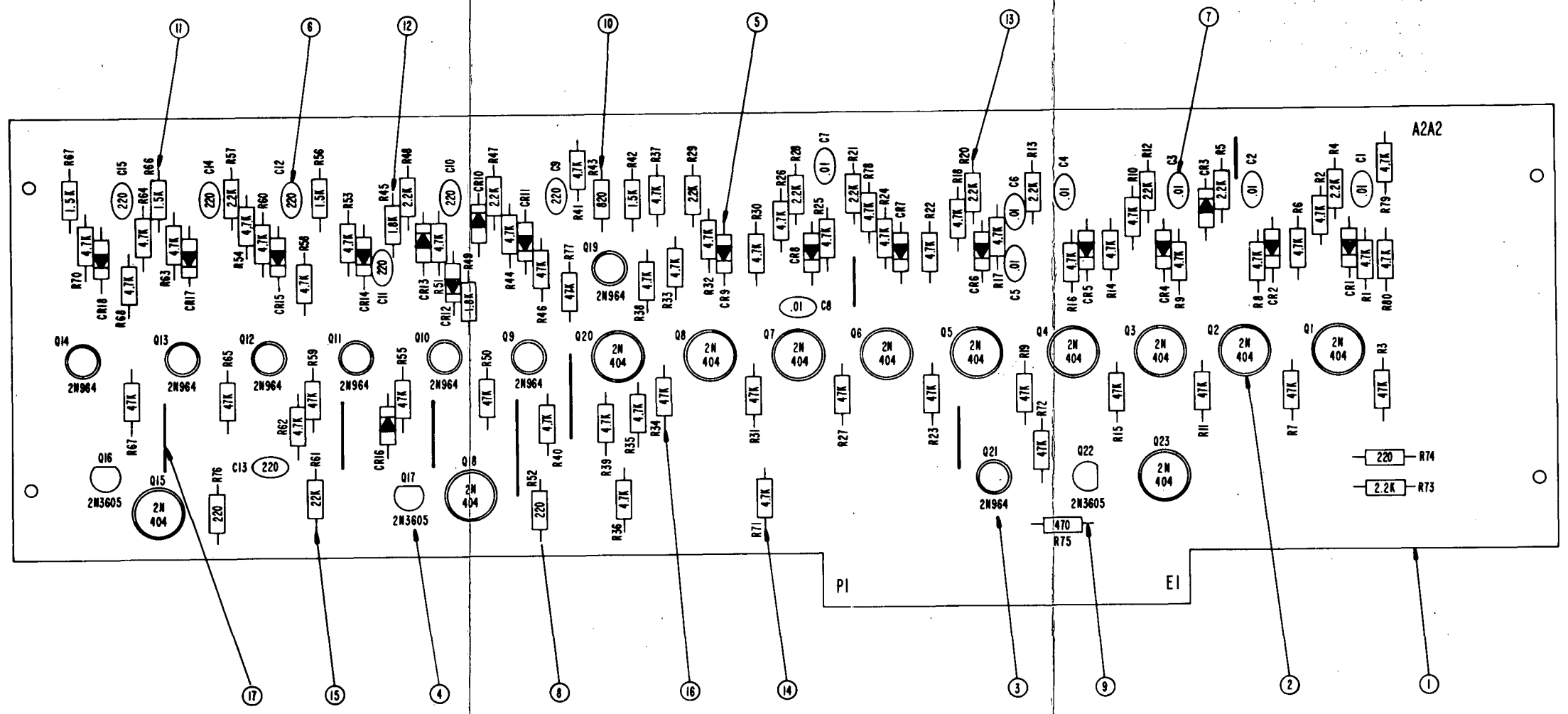
1. REFERENCE DESIGNATORS ARE ABBREVIATED FOR COMPLETE NUMBER PREFIX DESIGNATOR WITH ASSEMBLY NO. A2A3 .
2. DRILL ALL COMPONENT MOUNTING HOLES Φ.60 DRILL, AND BOARD MOUNTING HOLES Φ.29 DRILL, UNLESS OTHERWISE NOTED .
3. REF. SCHEMATIC D0070 .

Figure 6-21. Variable Frequency Oscillator and Decade Counter No. 1 Assembly Diagram

FOLDOUT FRAME

FOLDOUT FRAME 2

ITEM	REQD	PART NO.	DESCRIPTION	MATL OR MFR
			LIST OF MATERIAL	
17	A/R		WIRE, SOLID, 22 AWG	ALPHA
16	17	RC07GF473K	RESISTOR 47K 1/4 W ±10%	A-B
15	1	RC07GF223K	22K	
14	39	RC07GF472K	4.7K	
13	12	RC07GF222K	2.2K	
12	2	RC07GF182K	1.8K	
11	4	RC07GF152K	1.5K	
10	1	RC07GF821K	820Ω	
9	1	RC07GF471K	470Ω	
8	3	RC07GF221K	RESISTOR 220Ω 1/4 W ±10%	A-B
7	8	5035Y5U103Z	CAPACITOR .01 μF 25 V	ERIE
6	7	831Z5F221K	CAPACITOR 220 PF 500 V	ERIE
5	18	1N270	DIODE	G.I.
4	3	2N3605	TRANSISTOR	G.E.
3	6	2N964	TRANSISTOR	T.I.
2	12	2N404	TRANSISTOR	G.E.
1	1	NP346	PC BOARD	F.E.C.



NOTES:

1. REFERENCE DESIGNATORS ARE ABBREVIATED, FOR COMPLETE NO. PREFIX DESIGNATOR WITH ASSEMBLY NO. A2A2.

2. REFERENCE SCHEMATIC D08711.

3. DRILL ALL COMPONENT MOUNTING HOLES ⌀ 60 DRILL, & BOARD MOUNTING HOLES ⌀ 29 DRILL.

Figure 6-22. Divider Circuits Assembly Diagram

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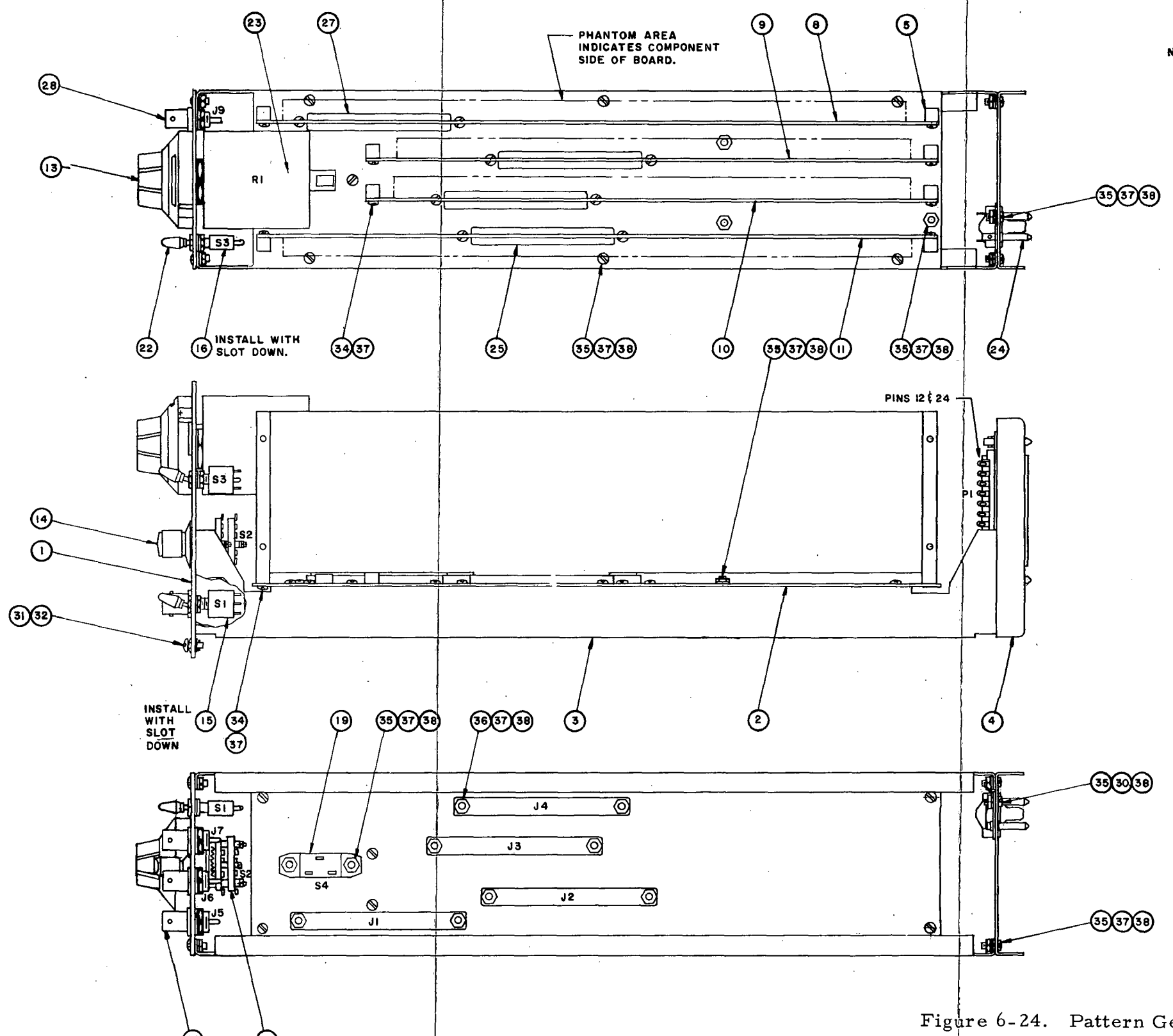
FOLDOUT FRAME 1

ITEM	REQD	PART NO	DESCRIPTION	MFR OR SPR
43	A/R	NO.13 GA	INSULATION, SLEEVING	ALPHA
42	A/R	NO.10 GA	INSULATION, SLEEVING	ALPHA
41	A/R	NO.22 GA	WIRE, ELEC. SOLID	ALPHA
40	A/R	NO.22 GA	WIRE, ELEC. INSULATING	ALPHA
39	A/R	3002 SIZE 24	TRANSFLEX TUBING, LACING	3M
38	31		NUT, NO.4-40 X 1/4 A F	BRASS
37	55		WASHER, NO.4 INT.TOOTH	
36	10		SCREW, NO.4-40 X 1/2 BD.HD.	
35	17		SCREW, NO.4-40 X 5/16 BD.HD.	
34	25		SCREW, NO.4-40 X 1/4 BD.HD.	
33	4		SCREW, NO.4-40 X 5/16 OVAL HD.	BRASS
32	2	5S3-2	WASHER, RETAINING	CAMLOC
31	2	5S27-9	STUD	CAMLOC
30	1	1418-4	SOLDER LUG	SMITH
29				
28	4	667-6	CONNECTOR	DAGE
27	1	251-15-30-160	CONNECTOR	CJ
26				
25	3	250-15-30-160	CONNECTOR	CJ
24	1	26-159-24	CONNECTOR	AMPHENOL
23	1	MODEL A	POTENTIOMETER, 10 TURN LINEAR, 50K .1%	HELIPOT
22	1	C-10	CAP (WHITE)	ALCO
21	2	PS-21	CERAMIC SECTION	CRL
20	1	P-505	INDEX ASSY.	CRL
19	1	G-324	SWITCH	CONT. WIRT
18				
17				
16	1	MST 105H	SWITCH	ALCO
15	1	MS1115D	SWITCH	ALCO
14	2	50-3-1G	KNOB	RAYTHEON
13	1	MODEL RB	KNOB, DUODIAL	HELIPOT
12				
11	1	D0907	ASSY. CRYSTAL OSC. & DIVIDER	F.E.C.
10	1	D0873	ASSY. VFO & DIVIDERS	
9	1	D0865	ASSY. DIVIDERS	
8	1	D0864	ASSY. SHIFT REGISTER GEN.	
7	1	B1019	BRACKET, MTG, PC BOARD	
6	1	B1018	PLUG HOLDER	
5	8	B0234	POST, MTG. PC BOARD	
4	1	B0423	CONNECTOR CHANNEL	
3	2	C0243	RAIL	
2	1	B1016	CHASSIS PLATE	F.E.C.
1	1	GEN-0231-028-	FRONT PANEL, ENGRAVED (NOTE 3)	GSFC

LIST OF MATERIAL

FOLDOUT FRAME 2



NOTES:
1. WIRING DIAGRAM D0919.
2. ASS'Y DESIGNATOR IS A2.
3. SPECIFY ONE OF THE FOLLOWING PAINT PART NOS:
   - 1 FST 595-26440 LIGHT GRAY
   - 2 GSDS GRAY
   - 3 SFOF BLUE

Figure 6-24. Pattern Generator Module Assembly Diagram

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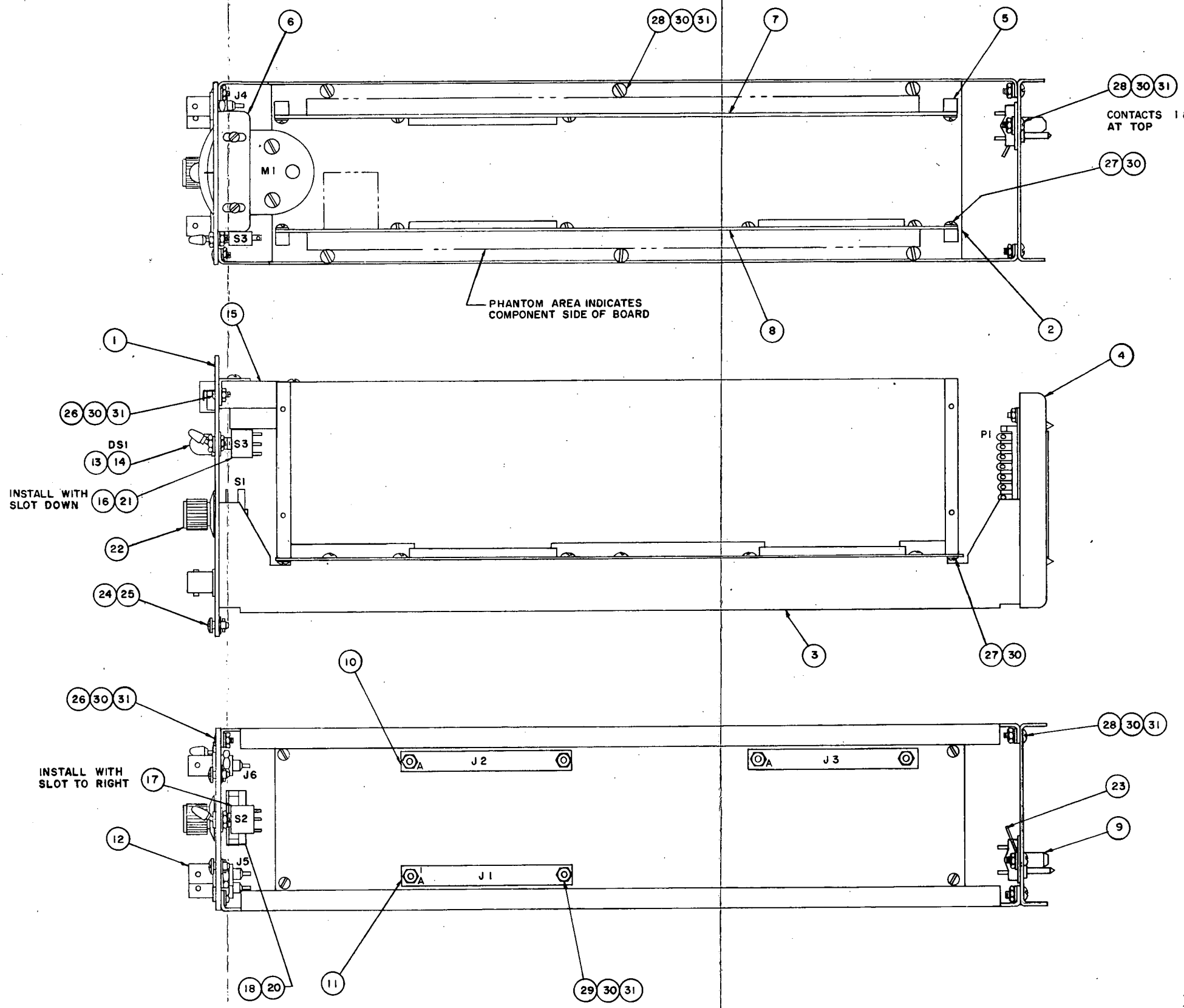
FOLDOUT FRAME 1



FOLDOUT FRAME 2

NOTES:

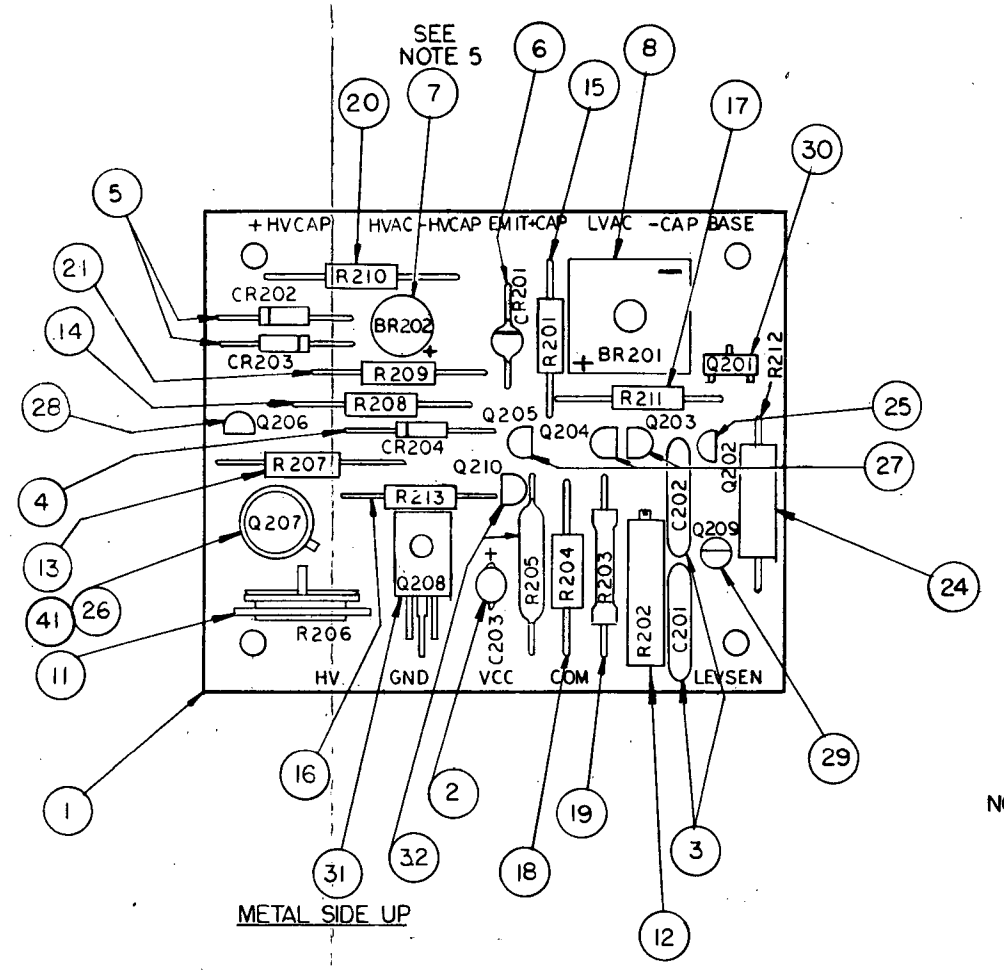
1. WIRING DIAGRAM D0917.
2. ASSEMBLY DESIGNATOR IS A5.
3. SPECIFY ONE OF THE FOLLOWING. PAINT PART NOS:
   - —4 FST 595-26440 LIGHT GRAY
   - —5 GSDS GRAY
   - —6 SFOF BLUE

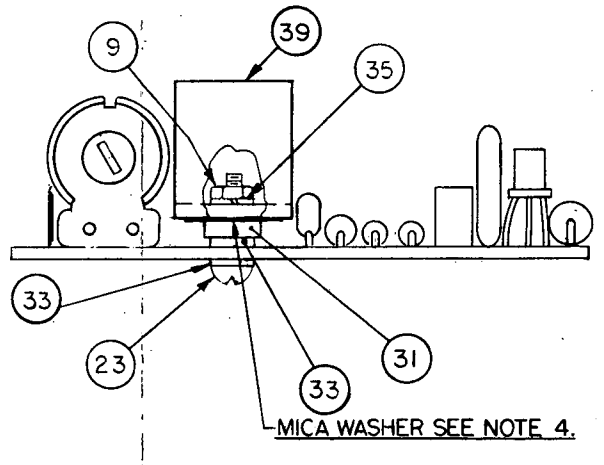
ITEM	QTY	PART NO	DESCRIPTION	MATL OR MFR
36	A/R	NO.22 GA	WIRE, ELEC. SOLID	ALPHA
35	A/R	NO.13 GA	INSULATION SLEEVING	ALPHA
34	A/R	NO.10 GA	INSULATION SLEEVING	ALPHA
33	A/R	NO.22 GA	WIRE, ELEC. INSULATED	ALPHA
32	A/R	3002 SIZE 24	TRANSFLEX TUBING LACING	3M
31	24		NUT, HEX NO.4 1/4 A F	BRASS
30	35		WASHER, NO.4 INT.TOOTH	"
29	6		SCREW, NO.4-40 X 1/2 BD.HD.	"
28	12		SCREW, NO.4-40 X 5/16 BD.HD.	"
27	12		SCREW, NO.4-40 X 1/4 BD.HD.	"
26	6		SCREW, NO.4-40 X 5/16 OVAL HD.	BRASS
25	2	5527-9	STUD	CAMLOC
24	2	553-2	WASHER,RETAINING	CAMLOC
23	1	1416-4	SOLDER LUG	H.H. SMITH
22	1	50-3-1G	KNOB	RAYTHEON
21	1	C-10	CAP, WHITE	ALCO
20	1	PA-115	CERAMIC SECTION	CRL
19				
18	1	P-505	INDEX ASSY.	CRL
17	1	MS215N	SWITCH	ALCO
16	1	MST105H	SWITCH	ALCO
15	1	MODEL 120	METER	TRIPLETT
14	1	327	LAMP BULB	G.E.
13	1	162-8430-931	LAMP ASSY. RED	DIALCO
12	3	667-6	CONNECTOR	DAGE
11	1	251-15-30-160	CONNECTOR	CJ
10	2	250-15-30-160	CONNECTOR	CJ
9	1	26-159-24	CONNECTOR	AMPHENOL
8	1	D0900	ASSY. INPUT & PHASE LOCK	FEC
7	1	N39079	ASSY. REC.PAT. SYNC & ERR DET.	WELEX
6	1	B0363	METER MTG. BRACKET	FEC
5	4	B0234	POST, MTG. PC BOARD	"
4	1	B0423	CONNECTOR CHANNEL	"
3	2	C0243	RAIL	"
2	1	B1010	CHASSIS PLATE	FEC
1	1	GEN-0231-028-	FRONT PANEL ENGRAVED (NOTE 3)	GSFC

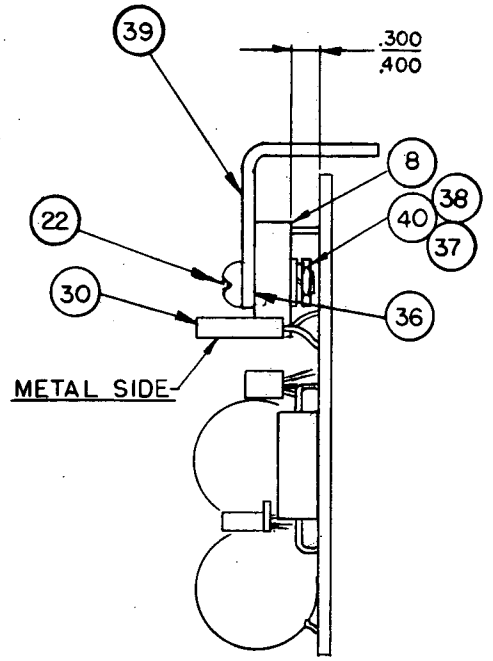
LIST OF MATERIAL

Figure 6-27. Receiver Module Assembly Diagram

FOLDOUT FRAME 1







NOTES:

1. ALL TRANSISTOR CENTER LEADS ARE BENT TOWARD FLAT SIDE EXCEPT Q203 AND Q204.
2. ASSEMBLE BR201 AND Q208 ASSYS AFTER WAVE SOLDERING. DO NOT OVER TIGHTEN.
3. HEATSINKS ARE NOT SHOWN ON TOP VIEW FOR CLARITY.
4. MICA WASHER SUPPLIED WITH Q208, APPLY THIN LAYER OF THERMAL GREASE (36) ON BOTH SIDES OF MICA WASHER.
5. BOTTOM OF BR202 TO BE 1/8 ABOVE P.C. BOARD COMPONENT SURFACE.

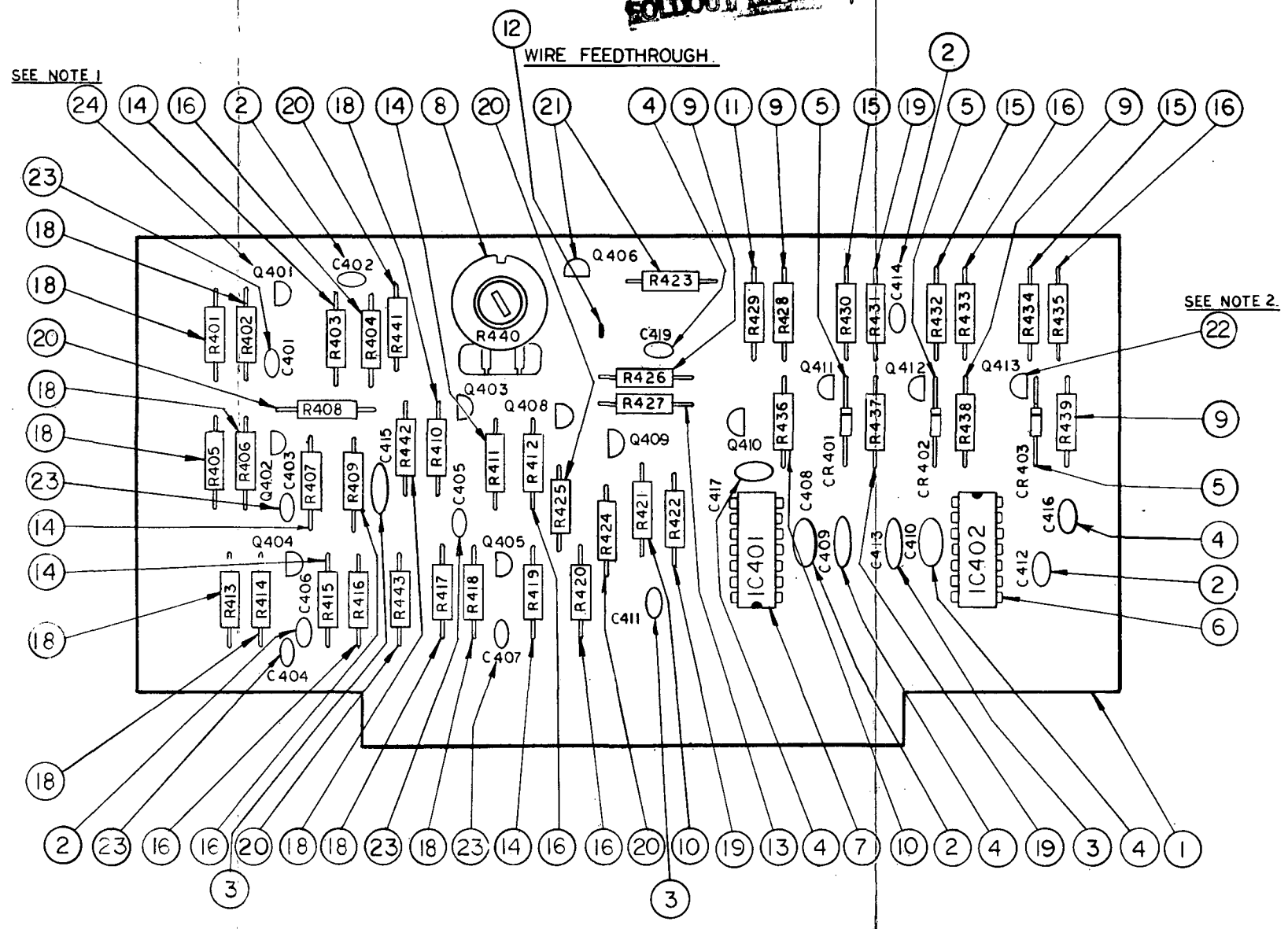
FOLDOUT FRAME 2

FIND NO	QTY. REQ'D	CAGE IDENT	IDENTIFYING NO.	DESCRIPTION	PART NUMBER	DRAWING NUMBER
				PARTS LIST		
41	1	13103	7717-22N	ISOLATOR	438-001-000-0	
40	1	96906	MS35338-136	WASHER	958-144-0004	
39	2			HEATSINK	391-016-000-2	391-016-000-2
38	1		6-32X1/16THK	NUT	558-05-01-001	
37	1	96906	MS15795-805	WASHER	957-156-0003	
36	A/R	05820	TYPE 122	GREASE: THERMAL	368-002-000-0	
35	1	96906	MS35338-135		958-118-0003	
33	2	83330	2161	WASHER	957-110-0001	
32	1			TRANSISTOR ASSY	929-1-000019	659-009-000-2
31	1	04713	MJE 340		929-3-000013	
30	1	04713	2N4918		929-3-000012	
29	1	03508	2N5172		929-2-000027	
28	1		2N5401		929-2-000026	
27	3		2N5089		929-2-000025	
26	1		2N2219A		929-2-000023	
25	1	04713	2N5457	TRANSISTOR	929-1-000012	
24	1	81349	RC42GF0R2J	RESISTOR .2Ω	715-0020-0-1-1	
23	1	96906	MS5I957-18	SCREW	78520-02-003	
22	1	96906	MS5I957-30	SCREW	787-16-02-001	
21	1	81349	RC20GF204J	200 K	715-2000-4-1-1	
20	1	81349	RC20GF621J	620Ω	715-6200-1-1-1	
19	1	75042	TYPE CES	549Ω	715-5490-1-4-1	
18	1	81349	RC20GF471J	470Ω	715-4700-1-1-1	
17	1	81349	RC20GF302J	3K	715-3000-2-1-1	
16	1		RC20GF754J	750K	715-7500-4-1-1	
15	1		RC20GF152K	1.5K	715-1500-2-1-2	
14	1		RC20GF135J	1.3M	715-1300-5-1-1	
13	1	81349	RC20GF103K	10K	715-1000-3-1-3	
12	1	73138	MOD 79P	VAR	706-5001-2-02	
11	1	71450	SER201,TYPEX-201	RESISTOR: VAR	706-2503-2-04	
9	1			NUT	556-01-01-001	
8	1	83003	VH148	DIODE: BRIDGE	267-6-000002	
7	1	83003	VE48	DIODE: BRIDGE	267-6-000001	
6	1	03508	A15F		267-5-000012	
5	2	81349	JANIN645		267-5-000001	
4	1	04713	IN5279	DIODE	267-3-000010	
3	2	81349	CK62AW472M	CAPACITOR 4700 pf	130-4706-002	
2	1	80183	196D106X0015EB	CAPACITOR 10 μf	130-1002-001	
1	1			BOARD	064-145-000-7	064-145-000-7

Figure 6-28. Power Supply Board Assembly Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2



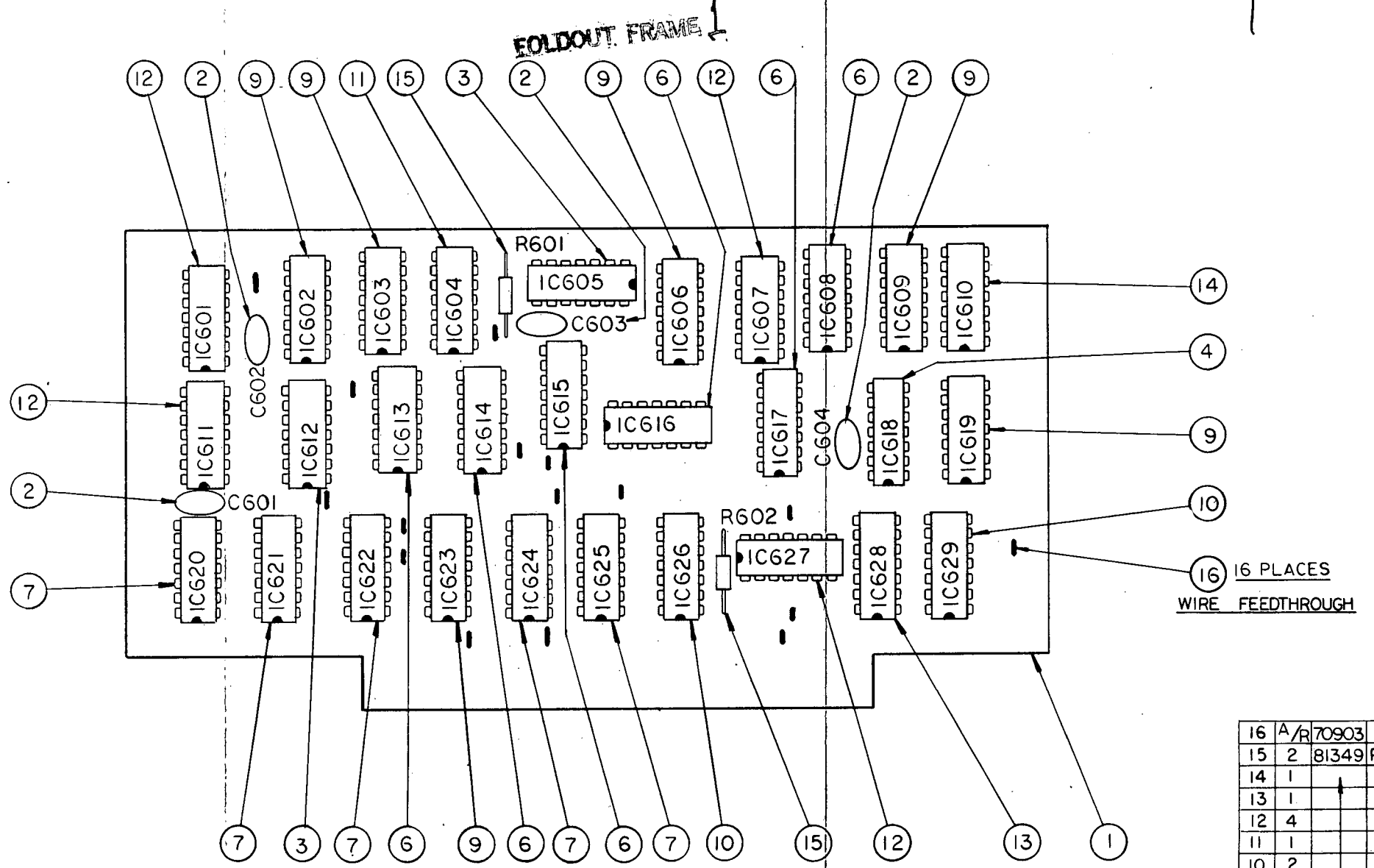
NOTES:
1. TRANSISTORS, Q401 THRU Q405 ARE 2N5227.
2. TRANSISTORS, Q408 THRU Q413 ARE 2N4124.

FIND NO.	QTY REQ'D	CODE IDENT	IDENTIFYING NO.	DESCRIPTION	PART NUMBER	DRAWING NUMBER
24	5	04713	2N5227	TRANSISTOR	929-2-000028	
23	5	71590	CE47J	CAPACITOR 470 pf	130-4707-002	
22	6	04713	2N4124	TRANSISTOR	929-2-000009	
21	1			TRANSISTOR ASSY	929-1-000020	659-010-000-3
20	5		RC20GF561K	560 Ω	715-5600-1-1-0	
19	3		RC20GF472K	4700 Ω	715-4700-2-1-2	
18	10		RC20GF471K	470 Ω	715-4700-1-1-3	
16	7		RC20GF272K	2.7 KΩ	715-2700-2-1-2	
15	3		RC20GF182K	1800 Ω	715-1800-2-1-2	
14	5		RC20GF822K	8.2K Ω	715-8200-2-1-2	
13	1	81349	RC20GF203J	RESISTOR 20 KΩ	715-2000-3-1-1	
12	A/R	70903	8021	WIRE 22AWG	980-1-22-0000-0	
11	1		RC20GF682K	6.8 KΩ	715-6800-2-1-2	
10	2		RC20GF103K	10 KΩ	715-1000-3-1-3	
9	4	81349	RC20GF102K	RESISTOR 1 KΩ	715-1000-2-1-5	
8	1	71450	U 201	RESISTOR, VAR 10 KΩ	706-1002-1-07	
7	1	18324	SN7400A	INTEGRATED CIRCIUT	432-675-0008	
6	1	04713	MC857P	INTEGRATED CIRCIUT	432-150-0001	
5	3	03508	IN4454	DIODE	267-5-000013	
4	5	80183	10TS-T22	220pf	130-2207-001	
3	3	71590	UK20-104	0.1μf	130-1004-004	
2	5	71590	UK10-104	CAPACITOR 0.1μf	130-1004-003	
1	1			BOARD	064-155-000-7	064-155-000-7

PARTS LIST

Figure 6-29. Translator Board Assembly Diagram

FOLDOUT FRAME 1



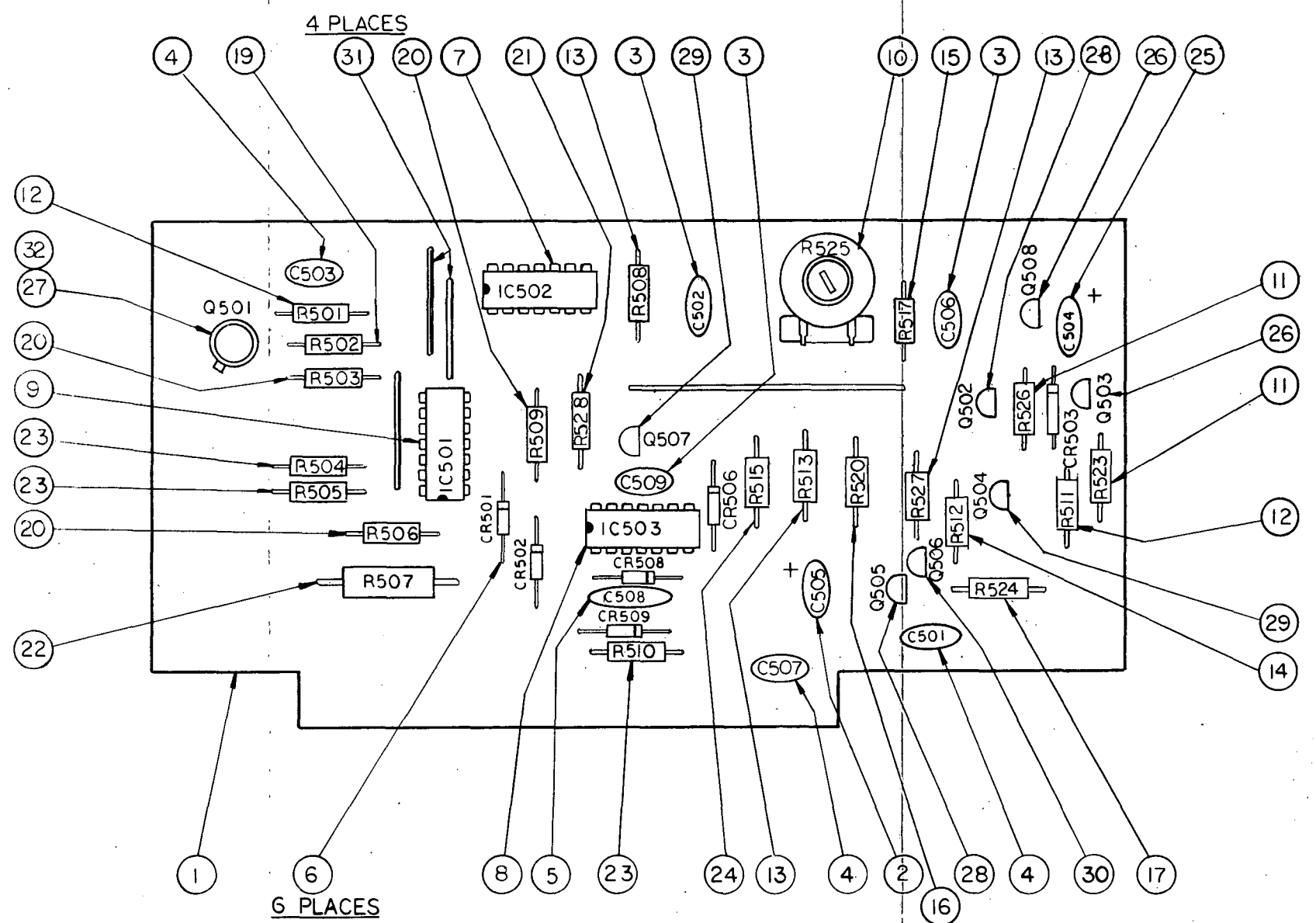
FOLDOUT FRAME 2

FIND NO.	QTY REQ'D	CODE IDENT	IDENTIFYING NO.	DESCRIPTION	PART NUMBER	DRAWING NUMBER
16	A/R	70903	8021	WIRE 22 AWG	980-1-22-00-00	
15	2	81349	RC07GF682J	RESISTOR 6.8 KΩ	715-6800-2-1-3	
14	1		SN7491A		432-900-0002	
13	1		SN7410A		432-675-0011	
12	4		SN7400A		432-675-0008	
11	1		SN7430A		432-675-0006	
10	2		SN7473A		432-375-0005	
9	6		SN7474A		432-375-0002	
7	5		SN7490A		432-225-0003	
6	6	18324	SN7493A		432-225-0002	
4	1	01295	SN74B6N		432-675-0007	
3	2	18324	SN7420A	INTEGRATED CIRCUIT	432-675-0004	
2	4	71590	UKI0-104	CAPACITOR 0.1μf	130-1004-003	
1	1			BOARD	064-153-000-7	064-153-000-7

PARTS LIST

Figure 6-30. Recognizer Board Assembly Diagram

FOLDOUT FRAME 1



FOLDOUT FRAME 2

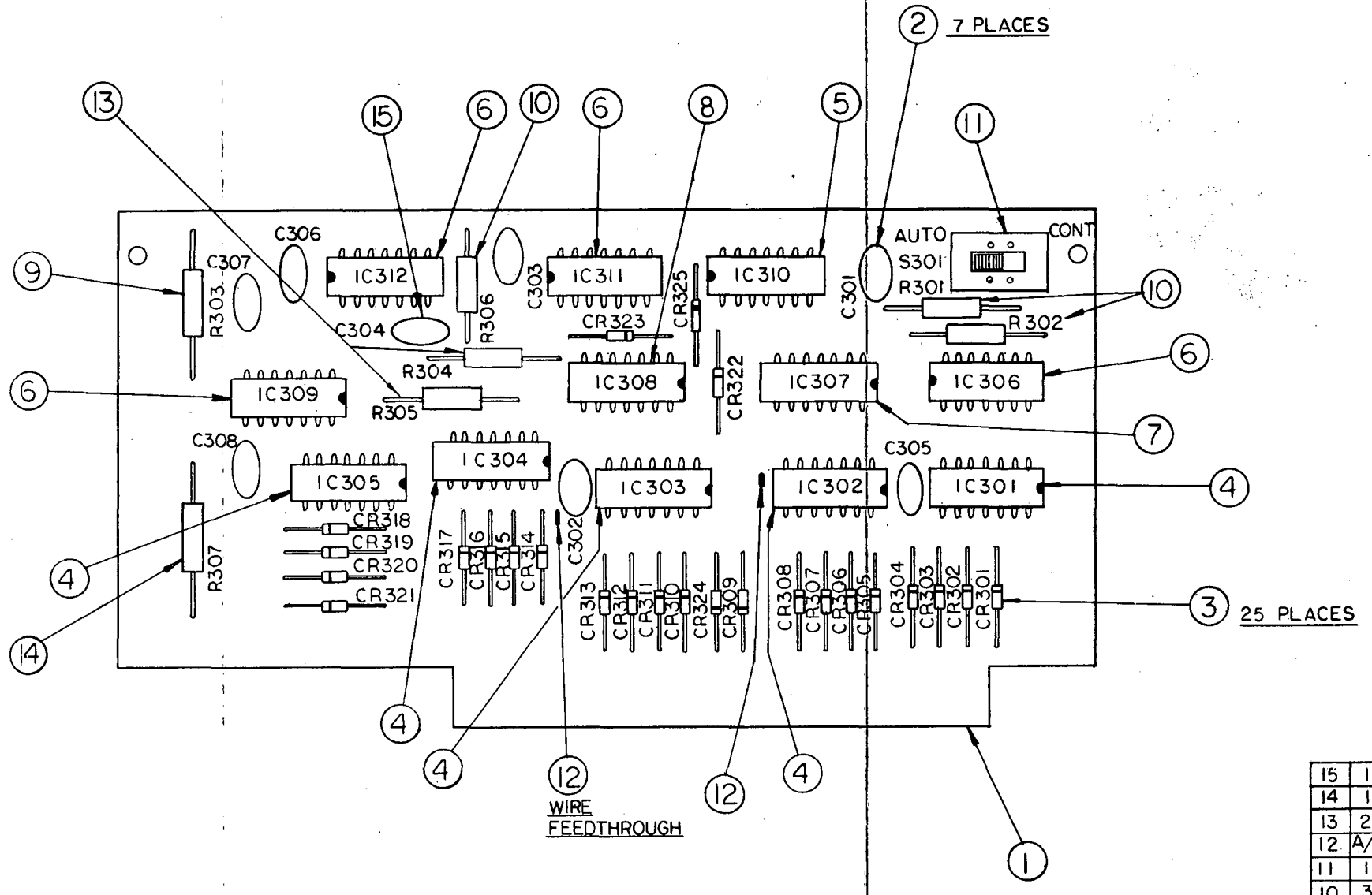
FIND NO.	QTY REQ'D	CODE IDENT	IDENTIFYING NO.	DESCRIPTION	PART NUMBER	DRAWING NUMBER
32	1	13103	7717-22N	ISOLATOR	438-001000-0	
31	A/R	70903	802	WIRE 22 AWG	980-1-22-0-C-0-0	
30	1	04713	2N4871		929-2-000029	
29	2	04713	2N5227		929-2-000028	
28	2	03508	2N5172		929-2-000027	
27	1	04713	2N2905A		929-2-000024	
26	2	04713	2N5457	TRANSISTOR	929-1-000012	
25	1	80183	196D156X0035EB	CAPACITOR 15 µf	130-1503-001	
24	1		RC20GF752J	7.5 KΩ	715-7500-2-1-1	
23	3		RC20GF682K	6800Ω	715-6800-2-1-2	
22	1		RC32GF470K	47Ω	715-4700-0-1-4	
21	1		RC20GF471K	470Ω	715-4700-1-1-3	
20	3		RC20GF331K	330Ω	715-3300-1-1-3	
19	1		RC20GF332K	3.3 KΩ	715-3300-2-1-0	
17	1		RC20GF101J	100Ω	715-1000-1-1-3	
16	1		RC20GF201J	200Ω	715-2000-1-1-2	
15	1		RC20GF243J	24KΩ	715-2400-3-1-1	
14	1		RC20GF102J	1 K Ω	715-1000-2-1-1	
13	3		RC20GF104K	100 KΩ	715-1000-4-1-3	
12	2		RC20GF103K	10 KΩ	715-1000-3-1-3	
11	2	81349	RC20GF105K	RESISTOR 1 MΩ	715-1000-5-1-3	
10	1	76055	MTC26L4	RESISTOR VAR 2MΩ	706-2004-1-01	
9	1	01295	MC858P		432-865-0001	
8	1	04713	MC840P		432-675-0003	
7	1	18324	SN7474A	INTEGRATED CIRCUIT	432-375-0002	
6	6	03508	IN4454	DIODE	267-5-000013	
5	1	81349	CK62AW427M	.0047 µf	130-4706-002	
4	3	71590	UK20-104	.1 µf	130-1004-004	
3	3	71590	UK10-104	0.1 µf	130-1004-003	
2	1	80183	196D106X0015EB	CAPACITOR 10 µf	130-1002-001	
1	1			BOARD	064-157-000-7	064-157-000-7

PARTS LIST

Figure 6-31. Outage Indicator Board Assembly Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

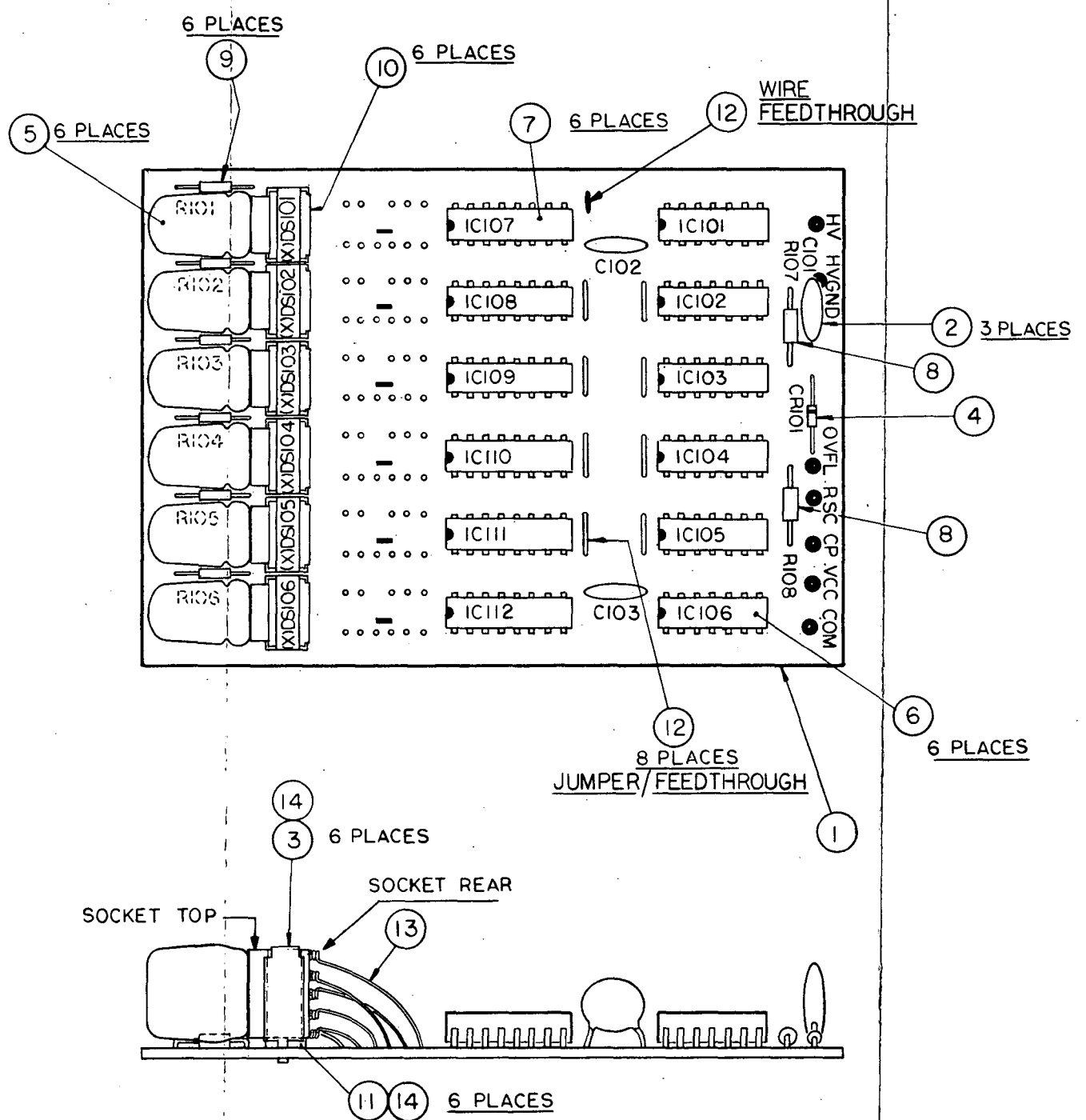


FIND NO.	QTY REQ'D	CODE IDENT	IDENTIFYING NO.	DESCRIPTION	PART NUMBER	DRAWING NUMBER
15	1	71590	CE47I	CAPACITOR 470 pf	130-4707-002	
14	1	81349	RC20GF470K	RESISTOR 47 Ω	715-4700-0-1-3	
13	2	81349	RC20GF222K	RESISTOR 2.2K Ω	715-2200-2-1-3	
12	A/R	70903	8021	WIRE 22 AWG	980-1-22-0-0-00	
11	1	79727	G-126PC	SWITCH	878-106-000-0	
10	3	81349	RC20GF682K	RESISTOR 6800 Ω	715-6800-2-1-2	
9	1	81349	RC20GF101K	RESISTOR 100 Ω	715-1000-1-1-4	
8	1	04713	MC840P		432-675-0003	
7	1		SN7410A		432-675-0011	
6	4		SN7400A		432-675-0008	
5	1		SN7474A		432-375-0002	
4	5	18324	SN7490A	INTEGRATED CIRCUIT	432-225-0003	
3	25	03508	IN4454	DIODE	2675-000013	
2	7	71590	UK10-104	CAPACITOR 0.1 μf	130-1004-003	
1	1			BOARD	064-149-000-7	064-149-000-7

PARTS LIST

Figure 6-32. Counter Display Control Board Assembly Diagram

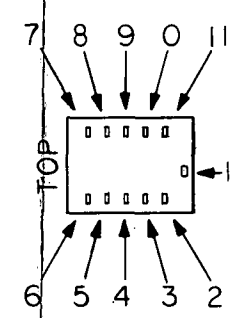
FOLDOUT FRAME 1



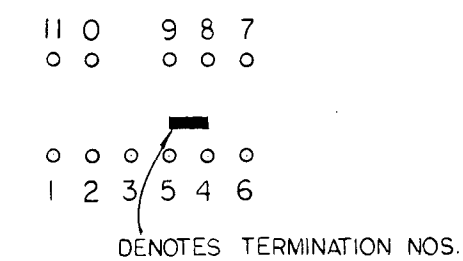
1

FOLDOUT FRAME 2

SOCKET TERMINATIONS AS VIEWED FROM REAR



SOCKET LEAD TERMINATION BOARD NUMBERS AS VIEWED FROM TOP



DENOTES TERMINATION NOS. 4 AND 5 ARE NOT IN SEQUENCE.

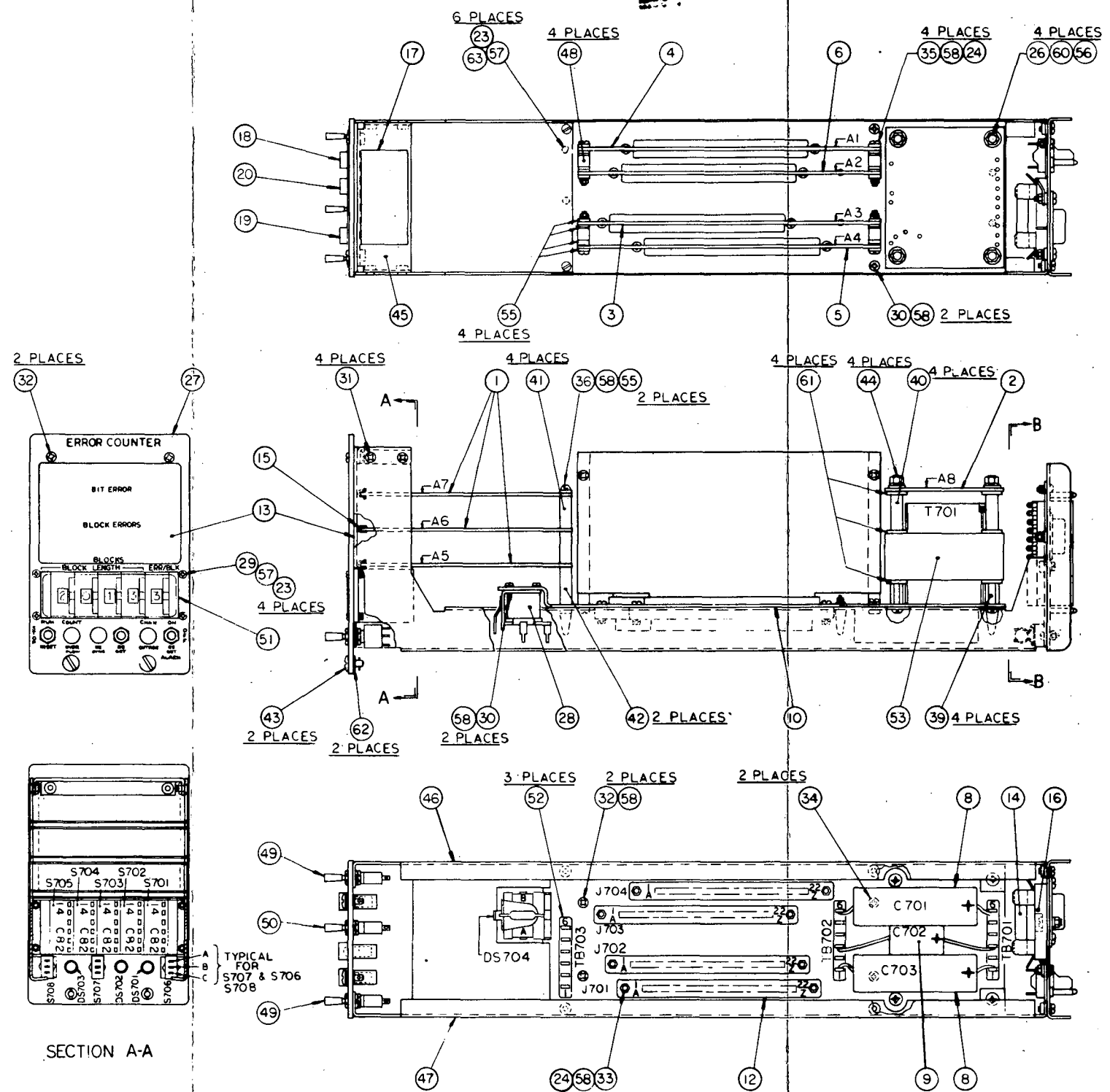
WIRING SOCKET TO BOARD		
SOCKET NO	BOARD NO	WIRE LENGTH
1	1	1 9/16
2	2	1 9/16
3	3	1 15/16
4	4	1 3/4
5	5	1 3/4
6	6	2
7	7	2
8	8	1 15/16
9	9	1 15/16
0	0	1 9/16
11	11	1 5/16

FIND NO.	QTY REQ'D	CODE IDENT	IDENTIFYING NO.	DESCRIPTION	PART NUMBER	DRAWING NUMBER
14	A/R	04633	2216 B-A	ADHESIVE	017-006-000-0	
13	A/R			WIRE 30 AWG	980-2306-00-1	
12	A/R			WIRE 22 AWG	980-1-22-0-0-00	
11	6			SPACER	844-073-000-2	844-073-000-2
10	6	08558	SK-178	SOCKET	836-005-000-0	
9	6	81349	RC07GF363J	RESISTOR 36 KΩ	715-3600-3-1-2	
8	2	81349	RC07GF104K	RESISTOR 100KΩ	715-1000-4-1-2	
7	6	18324	SN7441B	INTEGRATED CIRCUIT	432-345-0001	
6	6	18324	SN7490A	INTEGRATED CIRCUIT	432-225-0003	
5	6	08558	B4998	INDICATOR	418-002-000-0	
4	1	03508	IN4454	DIODE	267-5-000013	
3	6			CLIP	182-028-000-3	182-028-000-3
2	3	71590	UK10-104	CAPACITOR 0.1 μf	130-1004-003	
1	1			BOARD	064-134-000-7	064-134-000-7

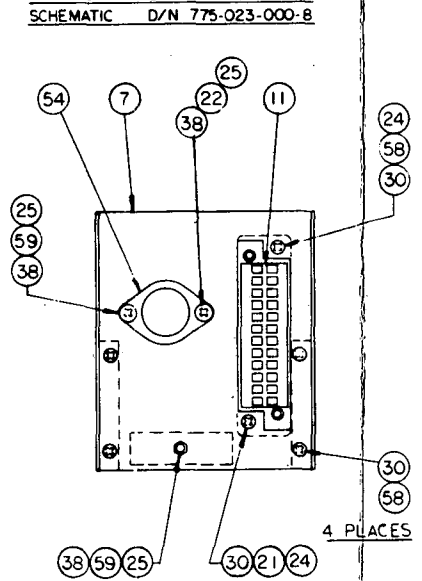
PARTS LIST

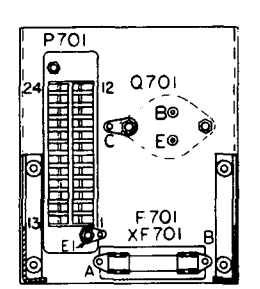
Figure 6-33. Counter Display Board Assembly Diagram

FOLDOUT FRAME 1



SECTION A-A





SECTION B-B

NOTE:

1. SPECIFY ONE OF THE FOLLOWING PAINTS:
   FST 595-26440, GRAY
   GSDS GRAY
   SFOF BLUE

REFERENCE DRAWINGS

WIRING LIST	D/N 982-006-000-3
SCHEMATIC	D/N 775-023-000-8

FOLDOUT FRAME 2

ITEM	QTY	REF DES	MFR CODE	VENDOR'S PART NO.	DESCRIPTION	PART NUMBER	DRAWING NUMBER
	1				MANUAL	422-013-000-0	
	1				BOARD ASSY, EXTENDER	064-150-000-3	064-150-000-3
63	6				WASHER	957-094-0001	
62	2		71286	553-2	RETAINING	361-011-000-0	
61	12				PIVOT	961-008-000-2	961-008-000-2
60	4			MS35338-137	"	958-170-0001	
59	2			MS35338-136	"	958-144-0004	
58	26			MS35338-135	"	958-118-0003	
57	16		96906	MS35338-134	"	958-091-0002	
56	4		86928	5602-76-62	FIBER	357-164-0001	
55	16		83330	2161	WASHER: FIBER	957-110-0001	
54	1		04713	2N3055	TRANSISTOR	929-3-000001	929-3-000001
53	1		07388	20456	TRANSFORMER	927-011-000-3	927-011-000-3
52	3		95146	MEP-6	TERMINAL STRIP	899-007-000-0	
51	1		97575	2000-30		878-109-000-0	
50	1		95146	MST105F		878-108-000-0	
49	2		95146	MST105H	SWITCH	878-107-000-0	
48	4					874-042-000-2	874-042-000-2
47	1					874-041-000-4	874-041-000-4
46	1					874-040-000-4	874-040-000-4
45	1				SUPPORT	874-039-000-3	874-039-000-3
44	4				SCREW 9-32	788-96-02-001	
43	2		71286	555-9	STUD	868-014-000-0	
42	2		83330	8721		844-077-000-0	
41	4		83330	8718		844-076-000-0	
40-44	3		83330	2128		844-075-000-0	
39	4		83330	8801	SPACER	844-108-000-0	
38	3		96906	MS51957-28	SCREW	787-12-02-003	
36	2				SCREW 4-40	785-89-06-001	
35	4				4-40	785-24-02-001	
34	2				4-40	785-16-08-001	
33	8		96906	MS51957-16		785-14-02-003	
32	4		96906	MS51957-15		785-12-02-001	
31	4				4-40	785-08-09-001	
30	10		96906	MS51957-26		785-08-02-004	
29	4				SCREW	784-10-02-004	
28	1		15447	10A111BB	RELAY	700-01-000-2	
27	1			NOTE 1	FRONT PANEL	596-108-000-3	
26	4		96906	MS35649-284		559-01-01-001	
25	3				6-32	558-05-01-001	
24	14				4-40	556-01-01-001	
23	10				NUT 2-56	559-01-01-001	
22	1		79963	502	LUG	479-004-000-0	
21	2		79963	75	LUG	479-001-000-0	
20	1		32539	L-6/50 AMBER	AMBER	466-004-000-0	
19	1		32539	L-6/50 RED	RED	466-002-000-0	
18	1		32539	L-6/50 WHITE	LIGHT WHITE	466-001-000-0	
17	1				LABEL	457-019-000-2	457-018-000-2
16	1		75915	357001	HOLDER	399-005-000-0	
15	3				HOLDER	397-012-000-2	397-012-000-2
14	1		75915	312001	FUSE	345-009-000-0	
13	1				FILTER	325-007-000-7	325-007-000-7
12	4		02660	225-2223-101	CONNECTOR	210-045-000-0	
11	1		02660	26-59-24	CONNECTOR	210-044-000-0	
10	1				CHASSIS	172-006-000-7	172-006-000-7
9	1		14655	TYPE BR4-450	CAPACITOR: 4 μF	130-4003-005	
8	2		80183	TL129	CAPACITOR: 1500 μF	130-151-001	
7	1				BRACKET	078-094-000-7	078-094-000-7
6	1					064-156-000-4	064-156-000-4
5	1					064-154-000-4	064-154-000-4
4	1					064-152-000-4	064-152-000-4
3	1					064-148-000-4	064-148-000-4
2	1					064-144-000-4	064-144-000-4
1	3				BOARD ASSY	064-135-000-4	064-135-000-4

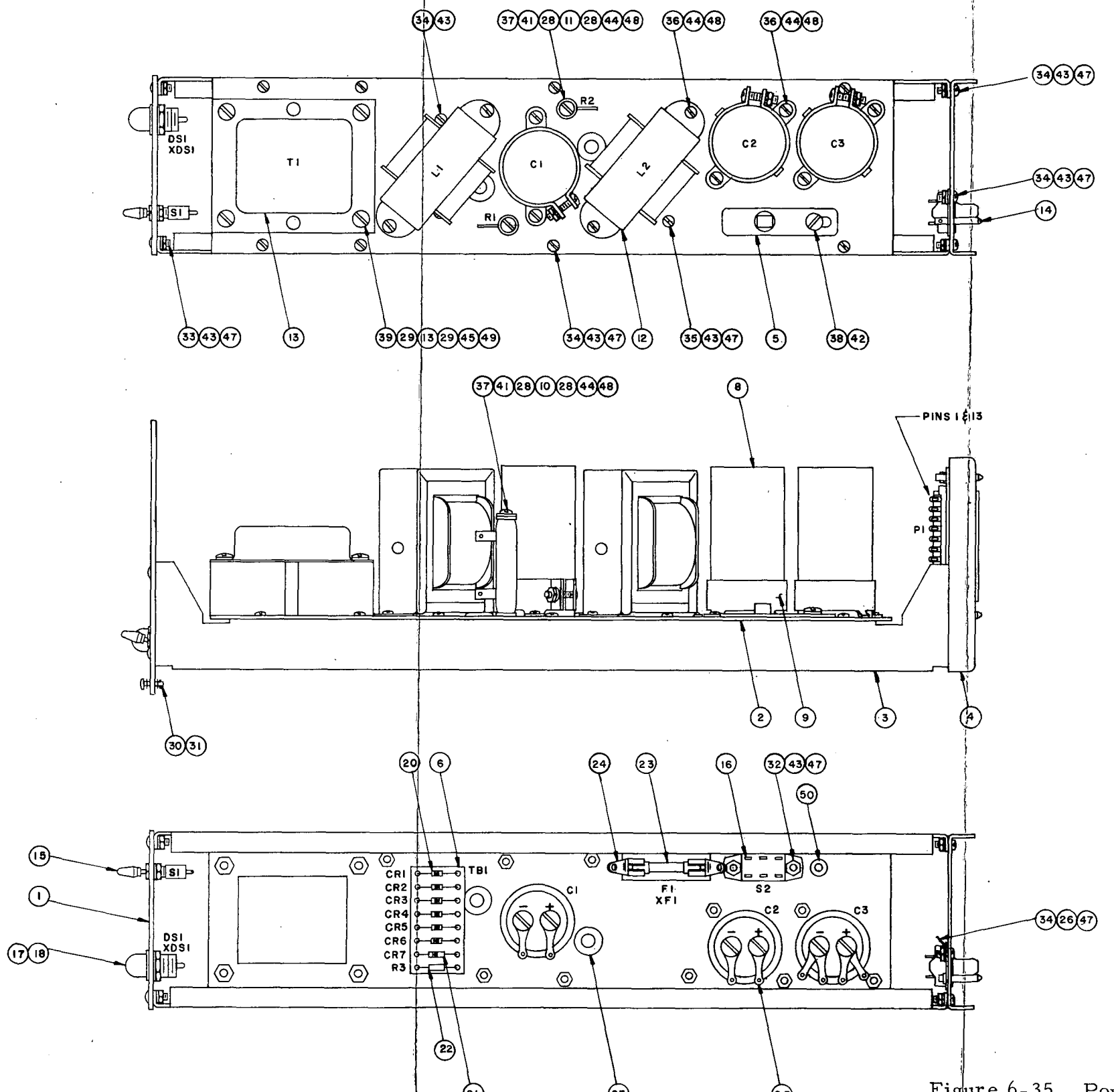
PARTS LIST

Figure 6-34. Error Counter Module Assembly Diagram

FOLDOUT FRAME 1

ITEM	REQD	PART NO.	DESCRIPTION	MATL OR MFR
			LIST OF MATERIAL	
57	A/R	NO.22 GA.	WIRE, ELEC, SOLID	ALPHA
56	A/R	NO.13 GA.	INSULATION, SLEEVING	ALPHA
55	A/R	NO.10 GA.	INSULATION, SLEEVING	ALPHA
54	A/R	NO.22 GA.	WIRE, ELEC, INSULATED	ALPHA
53	A/R	NO.18 GA.	WIRE, ELEC, INSULATED	ALPHA
52	A/R	3002, SIZE 24	TRANSFLEX TUBING, LACING	3M
51				
50	1	8-32-.050	CLINCH NUT	LAMPSON
49	4		NUT, HEX, NO.8-32 X 5/16 A.F.	BRASS
48	12		NUT, HEX, NO.6-32 X 1/4 A.F.	
47	21		NUT, HEX, NO.4-40 X 1/4 A.F.	
46				
45	4		WASHER, NO.8 EXT. TOOTH	
44	12		WASHER, NO.6 INT.TOOTH	
43	22		WASHER, NO.4 INT.TOOTH	
42	1		WASHER, NO.8 FLAT	
41	2		WASHER, NO.6 FLAT	
40				
39	4		SCREW, NO.8-32 X 1-1/2 BD. HD.	
38	1		SCREW, NO.8-32 X 5/16 BD. HD.	
37	2		SCREW, NO.6-32 X 2-1/4 BD. HD.	
36	10		SCREW, NO.6-32 X 5/16 BD. HD.	
35	1		SCREW, NO.4-40 X 3/8 BD. HD.	
34	16		SCREW, NO.4-40 X 5/16 BD.HD.	
33	4		SCREW, NO.4-40 X 5/16 OVAL HD.	
32	2		SCREW, NO.4-40 X 5/16 FLAT HD.	BRASS
31	2	553-2	WASHER, RETAINING	CAMLOC
30	2	5527-9	STUD ASS'Y	CAMLOC
29	8	2163	WASHER, FIBRE, NO.8	SMITH
28	4	2162	WASHER, FIBRE, NO.6	SMITH
27	2	2170	GROMMET	SMITH
26	1	1416-4	SOLDER LUG	SMITH
25	8	1416-8	SOLDER LUG	SMITH
24	1	4405	FUSE HOLDER	LITTELFUSE
23	1	313 3AG 1/2A	FUSE (SLO-BLO)	LITTELFUSE
22	1	RC07GF101K	RESISTOR, 100Ω, 1/4 W. 10%	A.B.
21	1	1N4838	DIODE	T.I.
20	6	1N4002	DIODE	T.I.
19				
18	1	327	BULB	G.E.
17	1	162-8430-932	LAMP ASS'Y (GREEN)	DIALCO
16	1	G-326	SWITCH	CONT.WIRT
15	1	MST 1150	SWITCH	ALCO
14	1	26-159-24	CONNECTOR	AMPHENOL
13	1	T1-895	TRANSFORMER	TRANSFORMERS INC.
12	2	T1-896	INDUCTOR	TRANSFORMERS INC.
11	1	3788	RESISTOR, 270Ω, 10 W	OHMITE
10	1	3764	RESISTOR, 27Ω, 10 W	OHMITE
9	3	CMC-22	CAPACITOR CLAMP	SPRAGUE
8	3	539-2536-6-01	CAPACITOR, TYPE DCM 4500 μF, 20 V	SANGAMO
7				
6	1	B1021	TERMINAL BOARD ASS'Y	F.E.C.
5	1	B1022	SWITCH PLATE	
4	1	B0423	CONNECTOR CHANNEL	
3	2	C0243	RAIL	
2	1	C1048	CHASSIS PLATE	
1	1	B1008 NOTE 4	FRONT PANEL ENGRAVED	F.E.C.

FOLDOUT FRAME 2



NOTES:
1. ASS'Y DESIGNATOR IS A5.
2. SCHEMATIC REF: C1050.
3. WIRING DIAGRAM REF: C1056.
4. SPECIFY ONE OF THE FOLLOWING PAINTS:
   FST 595-26440, GRAY
   GSDS GRAY
   SFOF BLUE

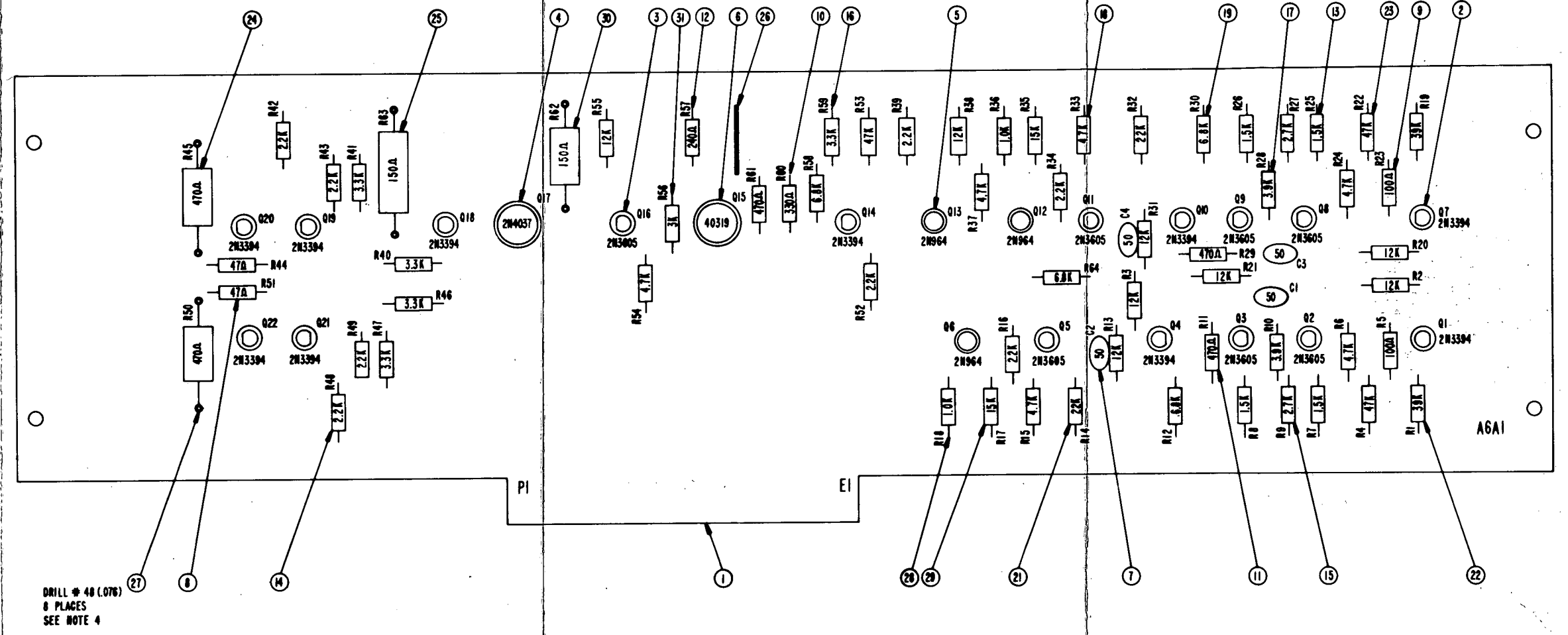
Figure 6-35. Power Supply Module Assembly Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

ITEM	REQ'D	PART NO.	DESCRIPTION	MFR
31	1	RC07GF302K	RESISTOR 3K, 1/4 W ±10%	MIL. STD.
30	1	RC32GF151K	RESISTOR 150Ω 1 W ±10%	MIL. STD.
29	2	RC07GF153K	RESISTOR 15K 1/4 W ±10%	MIL. STD.
28	2	RC07GF102K	RESISTOR 1.0K 1/4 W ±10%	MIL. STD.
27	8	2959	EYELETS	STIMPSON
26	A/R		WIRE, SOLID 22 AWG	ALPHA
25	1	RC32GF151K	RESISTOR 150Ω 1 W ±10%	A-B
24	2	RC20GF471K	RESISTOR 470Ω 1/2 W ±10%	A-B
23	3	RC07GF473K	RESISTOR 47K 1/4 W ±10%	A-B
22	2	393K	39K	
21	2	223K	22K	
20	8	123K	12K	
19	4	682K	6.8K	
18	6	472K	4.7K	
17	2	392K	3.9K	
16	5	332K	3.3K	
15	2	272K	2.7K	
14	8	222K	2.2K	
13	4	152K	1.5K	
12	1	241K	240Ω	
11	3	471K	470Ω	
10	1	331K	330Ω	
9	2	101K	100Ω	
8	2	RC07GF470K	RESISTOR 47Ω 1/4 W ±10%	A-B
7	4	831U2M500K	CAPACITOR 50 PF 600 V	ERIE
6	1	40319	TRANSISTOR	RCA
5	3	2N964		T.I.
4	1	2N4037		RCA
3	7	2N3605		G.E.
2	10	2N3394	TRANSISTOR	G.E.
1	1	NO330	PC BOARD	F.E.C.

LIST OF MATERIAL



NOTES:

1. REFERENCE DESIGNATORS ARE ABBREVIATED, FOR COMPLETE BOARDER PREFIX DESIGNATOR WITH ASSEMBLY NUMBER A6A1.
2. DRILL ALL COMPONENT MOUNTING HOLES WITH NO. 60 DRILL, AND BOARD MOUNTING HOLES WITH NO.29 DRILL.
3. SCHEMATIC REF. D0674
4. MOUNT 1 WATT AND 1/2 WATT RESISTORS WITH 1/8" CLEARANCE BETWEEN RESISTOR AND P.C. BOARD.

Figure 6-36. Data Set Adapter Converters Assembly Diagram

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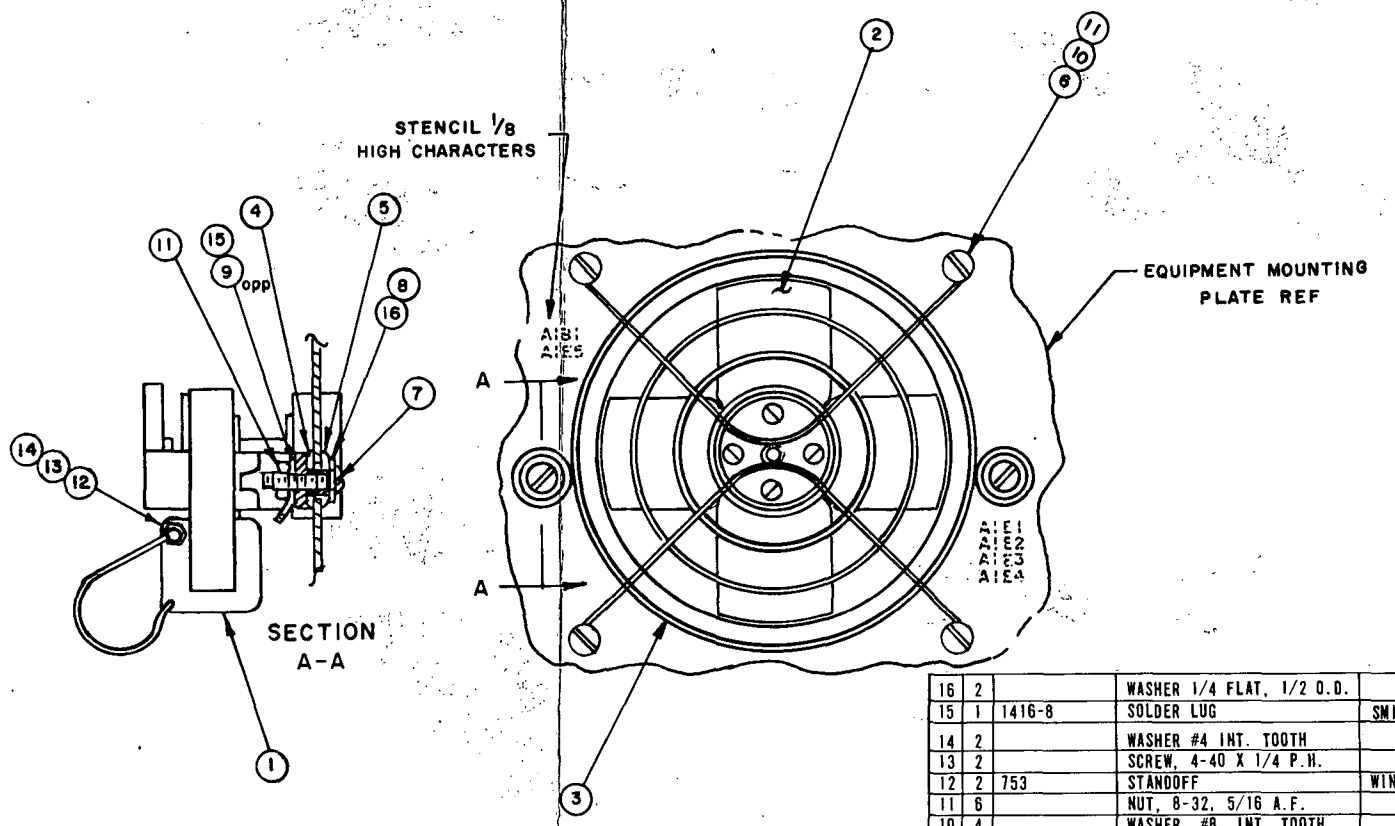

NOTE:

1 ADD JUMPER WIRE FROM 15, SOLDER LUG TO GROUND AT AC POWER INPUT.

ITEM	REQD	PART NO.	DESCRIPTION	MATL. OR MFR.	MATL. SPEC OR CAT. PART NO.	FINISH	FINISH SPEC	CKT SYM
16	2		WASHER 1/4 FLAT, 1/2 O.D.			NI		
15	1	1416-8	SOLDER LUG	SMITH				
14	2		WASHER #4 INT. TOOTH		STEEL	NI		
13	2		SCREW, 4-40 X 1/4 P.H.		STEEL	NI		
12	2	753	STANDOFF	WINCH				
11	6		NUT, 8-32, 5/16 A.F.		STEEL	NI		
10	4		WASHER, #8, INT. TOOTH					
9	1		WASHER, #8, SPLIT LOCK					
8	2		WASHER, #8, FLAT, 1/2 O.D.					
7	2		SCREW, 8-32 X 5/8 P.H.		STEEL	NI		
6	4		SCREW, 8-32 X 5/16 P.H.		STEEL	NI		
5	2	2170	GROMMET	SMITH				
4	2	80772	SPACER	FEC				
3	1	6-182-042	GUARD	HOWARD				
2	1	6-218-152	BLADES	HOWARD				
1	1	1075-08-3439	MOTOR	HOWARD				

LIST OF MATERIAL

Figure 6-39. Fan Installation and Assembly Diagram

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APPENDIX A

GLOSSARY OF LOGIC TERMS

AND

MODEL 1225 ERROR COUNTER MODULE LOGIC SYMBOLS

A. 1 GLOSSARY OF LOGIC TERMS

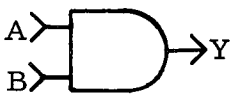
The following are definitions of logic terms used in discussion of operating principles of the Model 1225 Error Counter Module.

AND Gate. This is a binary circuit having two or more inputs and a single output. The output is "true" only if all inputs are "true" and "false" if any one of the inputs is "false."

AND Logic Statement:

$A \cdot B = Y$

AND Logic Diagram:



Truth Table

A	B	Y
F	F	F
F	T	F
T	F	F
T	T	T

Figure A-1. AND Gate

Bar $\overline{X}$. This is a symbol used to show the inverse or complement of a function.

BCD. This is an abbreviation for "binary coded decimal."

Buffer. A non-inverting member of the digital family which may be used to handle a large fan-out or to convert input and output levels. This also functions as an isolation stage at the input or output of a digital circuit.

Carry. This is a signal generated during addition of two binary digits when their sum exceeds the radix two.

Clear. This is the setting of one or more memory elements to a fixed state, generally, the "zero" or "false" state. This term is used interchangeably with "reset."

Clock. This is a continuous series of pulses which vary at a fixed frequency between logical "true" and logical "false." This signal serves to synchronize the logic system to which it is applied.

Exclusive-OR Gate (X-OR Gate). This is a binary circuit having two or more inputs and a single output. In this circuit, the output is "true" if any one of the inputs is "true", and the output is "false" if either the inputs are all "true" or all "false."

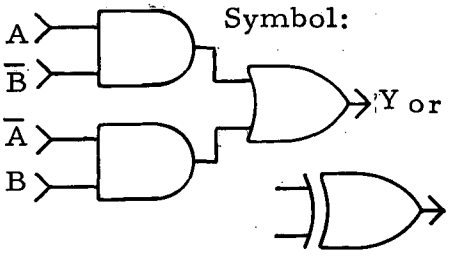
X-OR Logic Statement:

$A\overline{B} + \overline{A}B = Y$

or

$A \oplus B = Y$

X-OR Logic Symbol Symbol:



Truth Table

A	B	Y
F	F	F
F	T	T
T	F	T
T	T	F

Figure A-2. X-OR Gate

False. This is defined as logical "0" in Boolean algebra using positive logic notation.

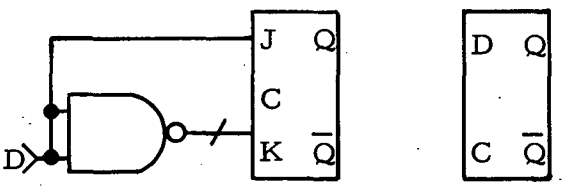
Fan-In. The total number of inputs of a particular gate or function.

Fan-Out. This is the total number of loads which are, or may be, connected to the output of a particular gate or function.

Flip-Flop. An electronic circuit having two stable states and the ability to change from one state to the other on application of a signal in a specified manner.

Flip-Flop, D. D stands for delay. This is a binary circuit having two inputs (D and clock) and two outputs (Q and $\overline{Q}$). When an input pulse is received at D, the Q output tracks the D input, synchronously with the clock.

D Flip-Flop Logic Diagram:



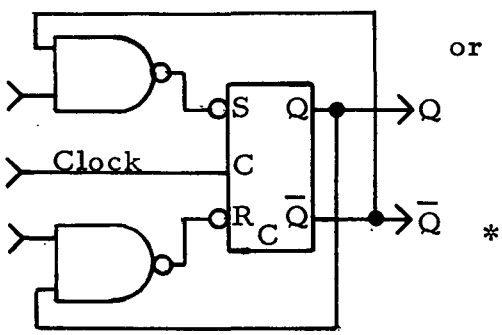
Truth Table

D	Q_{n+1}
F	F
T	T

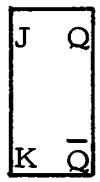
Figure A-3. D Flip-Flop

Flip-Flop, J-K. A flip-flop having two inputs designated J and K. This is a clocked R-S flip-flop which has the added characteristic of shifting from one output state to the other when it receives a "true" enable pulse on each input, or holding its present state when both inputs are "false."

J-K Flip-Flop
Logic Diagram:



or



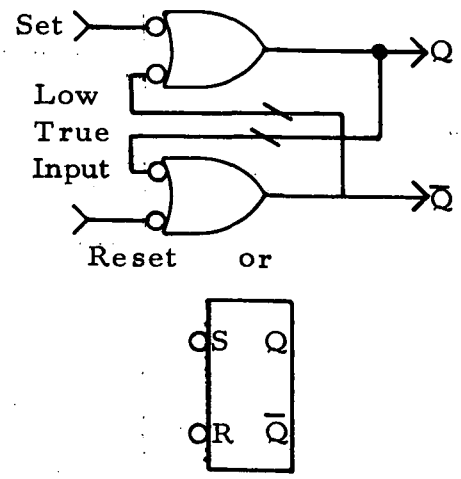
Truth Table

J	K	Q_{n+1}*
F	T	F
T	F	T
T	T	$\overline{Q}_n$

* Q_{n+1} is the output state of the flip-flop one clock pulse after the input combination appears.

Figure A-4. J-K Flip-Flop

Flip-Flop, R-S. A flip-flop having two inputs designated R and S. This is the basic set/reset flip-flop.



Truth Table

Previous State		Condition		Result	
Q	$\overline{Q}$	Set	Reset	Q	$\overline{Q}$
F	T	T*	F*	T	F
T	F	F*	T*	F	T
F	T	F*	F*	no change	
T	F	F*	F*	no change	
T	F	T*	F*	no change	
F	T	F*	T*	no change	
F	T	T*	T*	#	#
T	F	T*	T*	#	#

*Inverse Logic
#Ambiguous State

Figure A-5. R-S Flip-Flop

Flip-Flop, R-S, Clocked. This is a R-S flip-flop which is clock-synchronized by the addition of a two input NAND gate to each of the set and reset inputs. One of the inputs of each NAND gate is tied to a common clock (C), the other is connected to the set and reset inputs.

Logic Diagram:

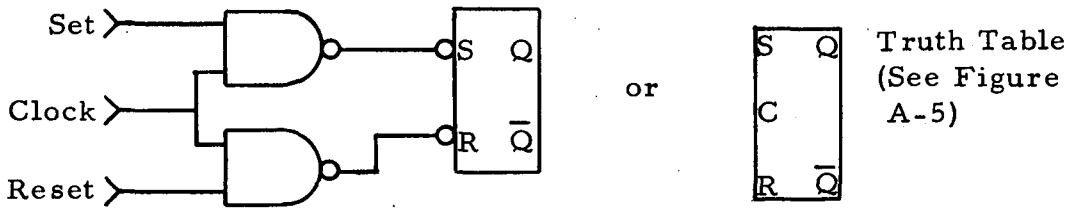
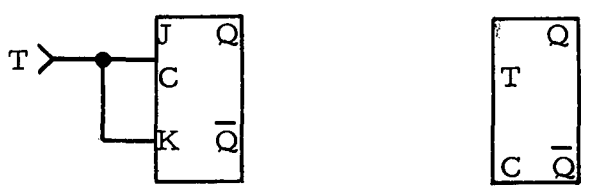


Figure A-6. Clocked R-S Flip-Flop

Flip-Flop, Toggled. This is a binary circuit which has two inputs (T and Clock), and two outputs (Q and $\overline{Q}$). When T is "true," the outputs Q and $\overline{Q}$ will shift to the complement of their previous state at each clock pulse. When T is "false," no change in the outputs Q and $\overline{Q}$ will occur.

Toggled Flip-Flop
Logic Diagram:



Truth Table

T	Q_{n+1}
F	Q_n
T	$\overline{Q}_n$

Figure A-7. Toggled Flip-Flop

Inverter. This is a binary circuit having a single input and a single output, in which the output is always the complement of the input. When the input is "high true," the output is "low true" and vice versa. Also called a NOT circuit.

Inverter
Logic Statement

$F = \overline{A}$

Inverter
Logic System

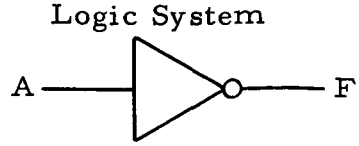


Figure A-8. Inverter

Latch. This is usually a feedback loop in a symmetrical digital circuit (such as flip-flop) for retaining a state.

Logic Levels. By convention, logical "1" is represented on a logic diagram by the most positive voltage level being used. This is positive logic which is referred to as "high true."

In certain applications it is necessary to redefine logical "1" and logical "0" thus making logical "1" a low voltage level (low true), and logical "0" a high voltage level. When this negative logic appears on a logic diagram, its employment is indicated by either a slash mark through the signal line or the generation of a signal line at a circle (See Figure A-9).

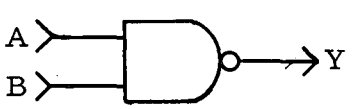
Figure A-9. Negative Logic Symbols

NAND Gate. This is a combination of an inverter and an AND gate. It is a binary circuit having two or more inputs and a single output. This output is "low true" only if all inputs are "true" and, conversely, is "false" if any one of the inputs is "false."

NAND Gate
Logic Statement:

$A \cdot B = \overline{Y}$

NAND Gate
Logic Diagram:



Truth Table

A	B	Y
F	F	F*
F	T	F*
T	F	F*
T	T	T*

*Negative Logic

Figure A-10. NAND Gate

OR Gate. This is a binary circuit having two or more inputs and a single output. When the output is "true," any one or all of the inputs are "true." When the output is "false," all inputs are "false."

OR Gate
Logic Statement:

A + B = Y

OR Gate
Logic Diagram:

Truth Table

A	B	Y
F	F	F
F	T	T
T	F	T
T	T	T

Figure A-11. OR Gate

Reset. This is the change in the output of a flip-flop from a "false" condition of $\overline{Q}$, to a "true" condition of $\overline{Q}$ using positive logic.

Set. This is the change in output of a flip-flop from a "false" condition of Q, to a "true" condition using positive logic.

Ripple Counter. This is an asynchronously controlled counter which has the clock signal derived from the output of a previous stage.

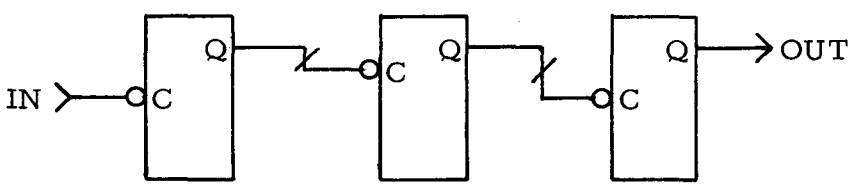


Figure A-12. Ripple Counter

Shift. This is the transfer of data from one memory device to another.

Shift Register. This is a storage device composed of n bits, with the ability to shift its stored data in one or the other direction.

Synchronous Operation. This is an operation which is controlled by a clock pulse.

True (T). This is defined as logical "1" in Boolean Algebra using positive logic notation.

Truth Table. This is a tabular list of all possible input logic combinations for a given function, together with the resulting output logic for all of these combinations.

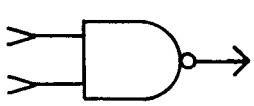
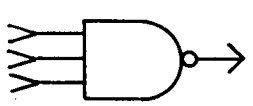
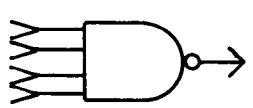
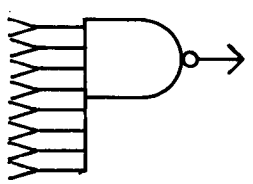
A. 2 ERROR COUNTER MODULE LOGIC SYMBOLS

Logic function symbols used in schematic diagrams of printed circuit boards in the Model 1225 Error Counter Module, together with type of devices employed to achieve given functions, are listed in the following paragraphs.

A. 2. 1 NAND GATES

Four types of NAND gates used in the error counter circuitry are listed in Table A-1.

Table A-1
NAND GATES

Type	Logic Symbol	Number of Inputs
7400 MC857 MC858		2
7410		3
7420		4
7430		8

A.2.2 INVERTERS

One type of inverter used in the error counter module is the MC840P. The inverter symbol used on schematic diagrams is shown in Figure A-13. The letter "X" within the symbol denotes no input diode in the inverter.

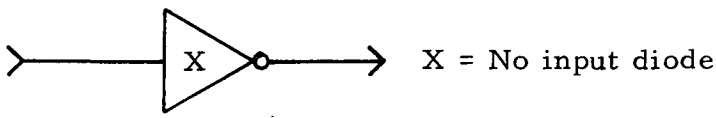


Figure A-13. Inverter Symbol

A.2.3 EXCLUSIVE-OR GATE

The error counter module uses a type 7486 device to achieve this function.

A.2.4 J-K FLIP-FLOP

A type 7473 device is used in the error counter module to achieve this function. Figure A-14 shows the input and output levels of this device. A master asynchronous reset input is used to override the J-K inputs.

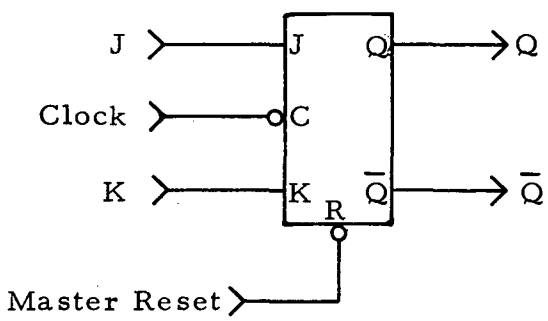


Figure A-14. J-K Flip-Flop Symbol

A.2.5 D FLIP-FLOP

A Type 7474 device is used to achieve this function. Figure A-15 shows the input and output levels. Both a master set and reset are

included which provide an asynchronous override over the D and clock inputs.

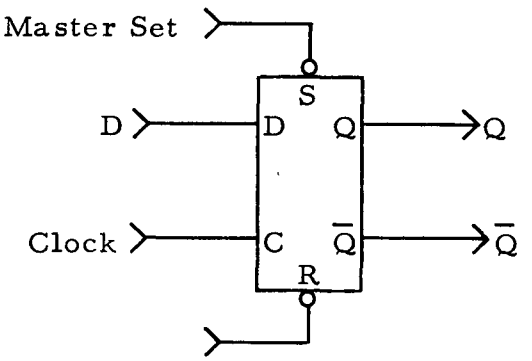


Figure A-15. D Flip-Flop Symbol

A. 2. 6 BCD TO DECIMAL DECODER/DRIVER

A type 7441B device is employed for the conversion of a four-line BCD code to a ten-line decimal code. In this device, buffer/drivers are included on the outputs for direct interfacing to the digital readout tubes. (See figure A-16)

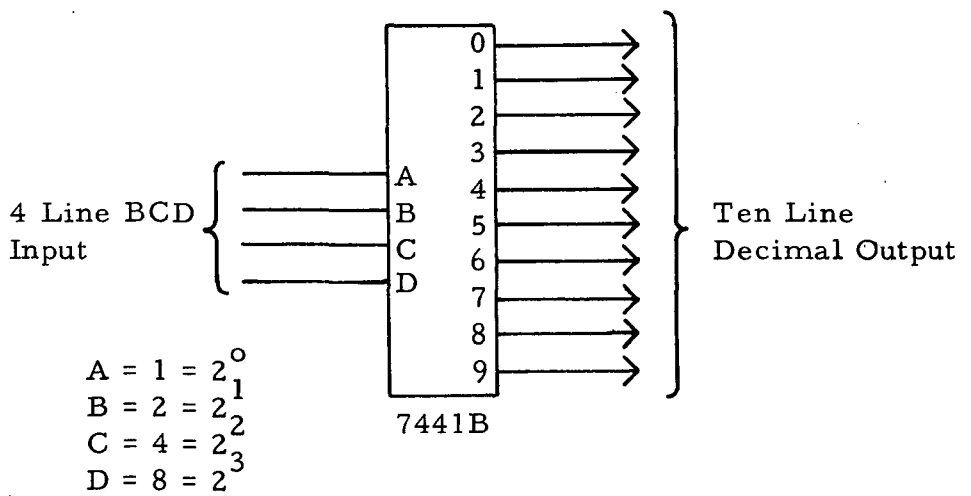


Figure A-16. BCD to Decimal Decoder/Driver Symbol

A. 2. 7 EIGHT BIT SHIFT REGISTER

This device is composed internally of eight R-S flip-flops connected so that binary data at the input is shifted to the output in eight clock pulses. A type 7491A device is used to perform this action. (See Figure A-17)

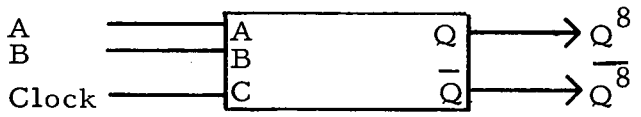


Figure A-17. Eight Bit Shift Register Symbol

A. 2. 8 DECADE COUNTER

A type 7490 device is used to perform this function. This device counts the input pulses and provides a running total from zero to nine in the binary output. Two master gated resets are provided for resetting the decade counter to either zero or nine. (See Figure A-18)

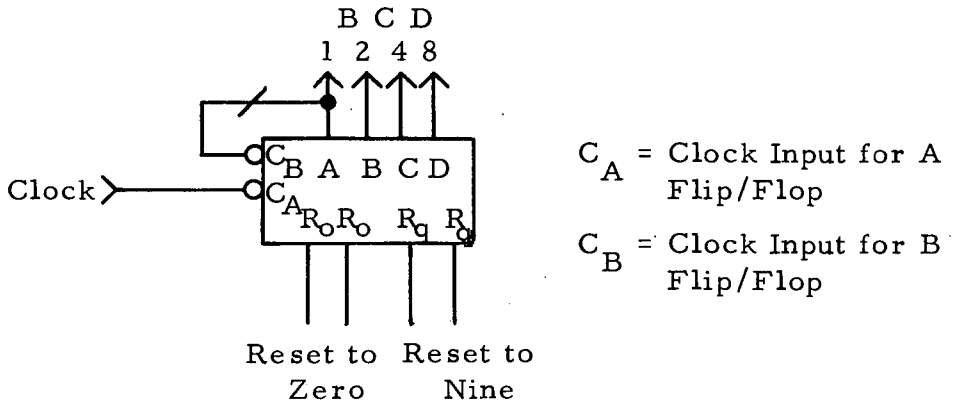


Figure A-18. Decade Counter Symbol

C-4

A. 2. 9 BINARY COUNTER

A type 7493 device is used to perform this function. This device counts the input pulses and provides a running total from zero to fifteen in the form of a binary output. A master gated reset is provided for reset of the binary counter to zero. (See Figure A-19)

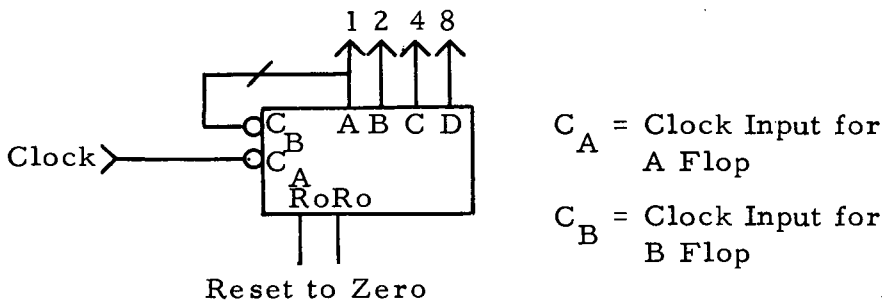


Figure A-19. Binary Counter Symbol

A. 2. 10 EDGE CATCHER

An edge catcher is a device for detecting, or "catching" a logic transition from either the "true" to "false" or the "false" to "true" logic states. The device used to perform this function is a type 7474 device. (See Figure A-20)

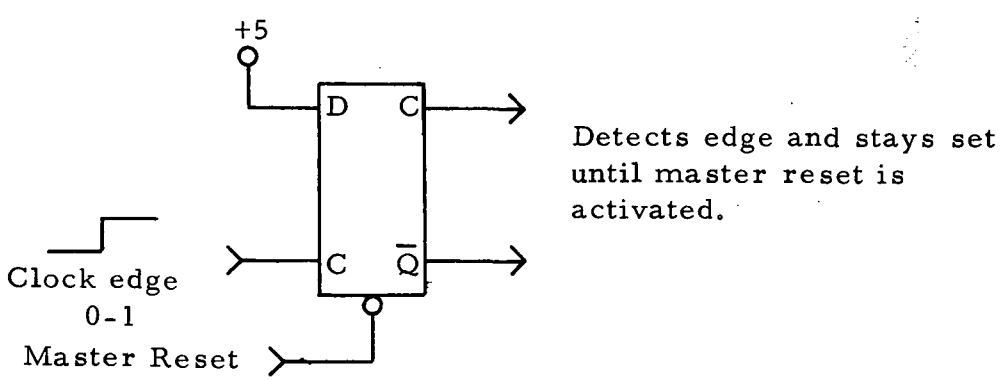


Figure A-20. Edge Catcher Symbol

APPENDIX B

INSTRUCTIONS FOR

MODEL 600 ERROR COUNTER MODULE

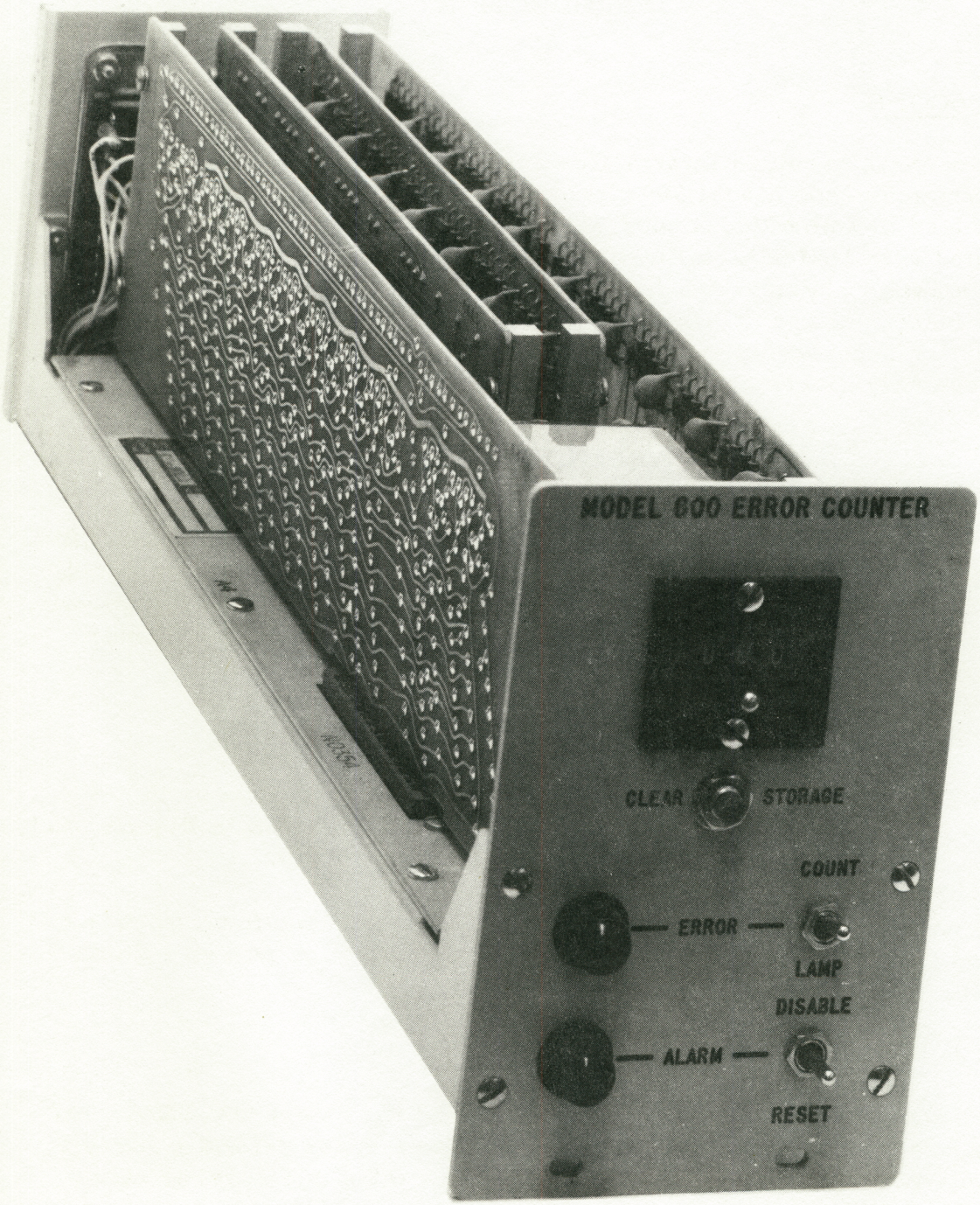


Figure B1-1. Model 600 Error Counter

SECTION B1

INTRODUCTION

B1.1 SCOPE

This appendix provides information necessary for the operation and maintenance of the Model 600 Error Counter Module (ECM) which is being used in some Model 600F Data Transmission Test Sets that are not equipped with Model 1225 ECM. This appendix contains a description of the equipment physical and functional characteristics; operating instructions; functional and detailed descriptions of principles of operation; preventive and corrective maintenance procedures; and block, schematic, and assembly diagrams.

B1.2 GENERAL DESCRIPTION

The Model 600 ECM is designed to store incoming error pulses developed in the receiver error detection circuit at rates as high as 100 kbs, and to register the total count at a slower rate on the front panel mechanical totalizer. It is provided with a visual and aural alarm system which issues a warning when the error rate exceeds the counter storage capacity.

B1.2.1 PHYSICAL DESCRIPTION

The Model 600 ECM is a plug-in module 3-3/8 inches wide by 5-1/8 inches high by 15-9/32 inches deep. The module, shown in Figure B1-1, is used in chassis position A4 of the Model 600F DTTS.

Electronic circuits are all solid-state, packaged in the form of plug-in printed circuit boards. Table B1-1 provides a list of printed circuit boards.

B1.2.2 FUNCTIONAL DESCRIPTION

Figure B1-2 is a simplified block diagram of the Model 600 ECM. Incoming error pulses developed in the receiver error detection circuit are applied to the high speed storage section (ring counters) at rates as high as 100 kbs. Because of mechanical limitation of the readout device, the readout rate cannot exceed 25 counts-per-second. The

Table B1-1

MODEL 600 ECM PRINTED CIRCUIT BOARDS

Board Reference No.	Description
NO351	4- and 5-Stage Ring Counters
NO352	7-Stage Ring Counter
NO353	Counter Control
NO354	11-Stage Ring Counter

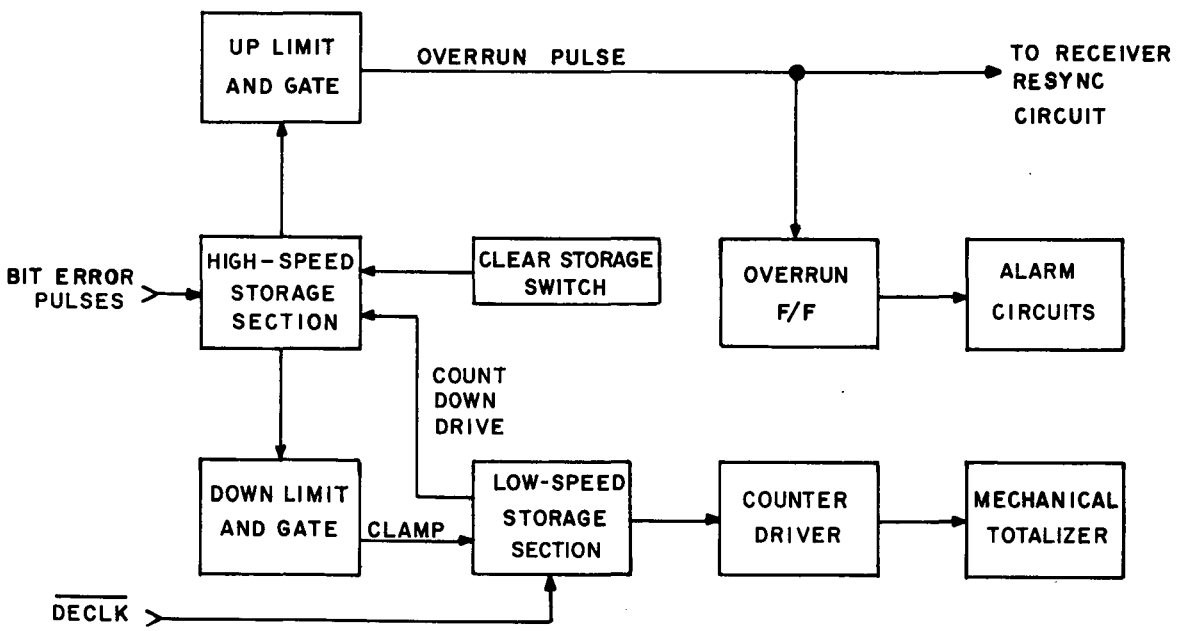


Figure B1-2. Model 600 Error Counter Module Simplified Block Diagram

high-speed ring counters accumulate the incoming errors, and the low speed section then accepts the errors through the down-limit AND gate and supplies them to the mechanical totalizer at a reduced rate. Whenever the 1540 bit storage capacity of the high speed storage section is exceeded, an overrun pulse is developed by the up-limit AND gate. This pulse is simultaneously applied to the receiver resynchronization circuit to initiate pattern resynchronization, and to the overrun flip-flop to turn on the alarm buzzer and indicator lamp. Delayed clock pulses from the receiver module are applied to the low-speed section to trigger the 20-millisecond one-shot in the counter control circuit. A front panel CLEAR STORAGE switch is used to reset the high speed storage section to the zero, or empty, state.

B1.3 EQUIPMENT CHARACTERISTICS

The electrical characteristics of the Model 600 ECM are listed in Table B1-2.

Table B1-2

ELECTRICAL CHARACTERISTICS

Characteristic	Value
Maximum Storage Capacity	1540 bits
Maximum Error Burst	1540 consecutive errors
Maximum Readout Rate	20 errors-per-second (average)
DC Power Input Voltages	±12 volts for ring counters, logic gates, and flip-flops
	+15 volts for mechanical totalizer and ERROR lamp
Error Pulse Input Level	Negative going, 0 volt to -12 volts
Delayed Clock Input Level	Negative going, 0 volt to -6 volts
Resync Pulse Output Level	Positive going, 0 volt to +12 volts

SECTION B2

INSTALLATION

The Model 600 Error Counter Module (ECM) is presently employed in Model 600F Data Transmission Test Sets (DTTS) that are not equipped with Model 1225 ECM. In DTTS units employing a Model 1225 ECM, the Model 600 ECM may be used as a back-up spare substitute for the Model 1225.

SECTION B3

OPERATION

B3.1 INTRODUCTION

This section describes front panel operating controls and indicators, and provides instructions necessary to operate the Model 600 Error Counter Module (ECM).

B3.2 CONTROLS AND INDICATORS

Figure B3-1 and Table B3-1 identify and describe the front panel controls and indicators on the Model 600 ECM. Control and indicator names presented in upper case letters in Table B3-1 are those placarded on the equipment. The name with initial capital letters has been assigned in the absence of a name placarded on the equipment.

B3.3 OPERATING PROCEDURES

The Model 600 ECM receives its dc operating voltages from the DTTS power supply module, and is ready for operation when the power supply module primary power switch is turned on. To operate the ECM, proceed as follows:

a. Depress front panel thumb lever on mechanical totalizer (M1) to reset display to zero.

b. Depress front panel CLEAR STORAGE pushbutton switch (S2) to reset high-speed electronic storage (ring counters) to zero or empty state.

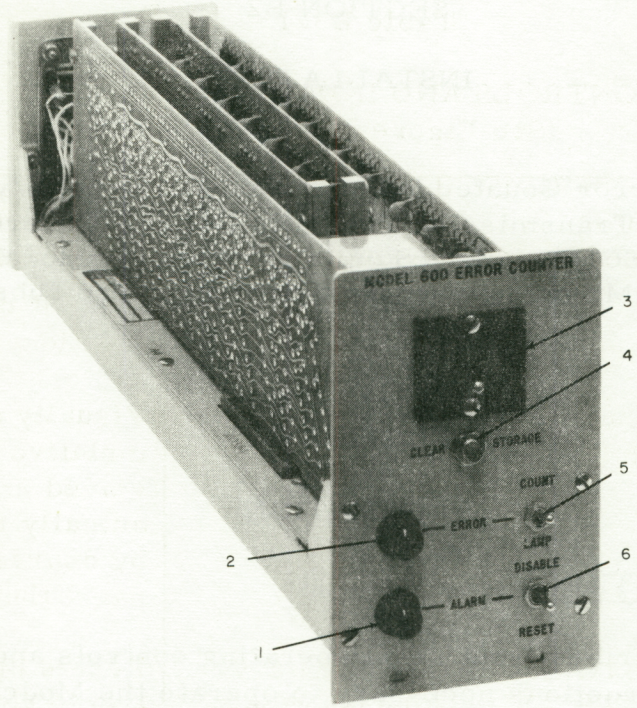


Figure B3-1. Controls and Indicators (Refer to Table B3-1)

Table B3-1

CONTROLS AND INDICATORS
(See Figure B3-1)

Index No.	Name	Type	Function
1	ALARM (DS2)	Indicator lamp	Lights to indicate that capacity of high-speed storage has been exceeded. An internal buzzer (DS1) is operated simultaneously with ALARM lamp
2	ERROR (DS3)	Indicator lamp	Flashes during error readout when COUNT-ERROR-LAMP (S3) switch is set to either

Table B3-1

CONTROLS AND INDICATORS (Cont)
(See Figure B3-1)

Index No.	Name	Type	Function
2 (Cont)			ERROR or LAMP position
3	Mechanical Error Totalizer (M1)	Mechanical count display	Visually displays cumulative total of received errors. Mechanically reset to zero by depressing front panel thumb lever
4	CLEAR STORAGE (S2)	Momentary pushbutton switch	Resets high speed electronic storage to zero as required during set-up or operational procedures
5	COUNT-ERROR-LAMP (S3)	3-position Toggle switch	Controls display of errors in each position, as follows: COUNT - Enables mechanical totalizer ERROR - Permits mechanical totalizer and ERROR lamp to function normally LAMP - Disables mechanical totalizer and permits ERROR lamp to flash during error readout

Table B3-1

CONTROLS AND INDICATORS (Cont)
(See Figure B3-1)

Index No.	Name	Type	Function
6	DISABLE-ALARM-RESET (S1)	3-position toggle switch	Controls operation of overrun alarm in each position, as follows: DISABLE - Disables ALARM lamp and buzzer circuits ALARM - Permits ALARM lamp and buzzer circuit to function normally RESET (momentary) - Resets ALARM lamp and buzzer circuits

c. Set front panel COUNT-ERROR-LAMP switch (S3) to either COUNT position or ERROR position. Mechanical totalizer should start counting error pulses developed in receiver error detection circuit.

d. Reset ECM as required during operation by repeating steps a and b.

SECTION B4

PRINCIPLES OF OPERATION

B4.1 INTRODUCTION

In this section, operation of the Model 600 Error Counter Module is described both at a functional level and at a circuit level. The functional description is keyed to the block diagram in Figure B6-1. The detailed circuit level description is keyed to the schematic diagrams in Section B6 of this manual.

B4.2 FUNCTIONAL DESCRIPTION

The error counter module contains a high-speed electronic storage section, a low-speed error readout section, and an overrun alarm section. The high-speed section consists of ring counters suitably arranged to store a maximum count of 1540 error bits; the low-speed error readout section accepts the error from the high-speed section and supplies them to a mechanical totalizer at a reduced rate; and the overrun alarm section activates a visual and aural alarm when the capacity of the high speed section is exceeded, and develops a resync pulse which is applied to the receiver module.

The error counter counts the number of error pulses from the error flip-flop in the receiver module and registers the total count on a front panel indicator. Although the rate of incoming error pulses can be as high as 100 kbs, the readout rate cannot exceed 25 counts-per-second due to mechanical limitation of the readout device. This large difference between input and output rates is buffered by the 1540 count capacity of the high-speed section.

B4.2.1 HIGH-SPEED ELECTRONIC STORAGE SECTION

Separately, the ring counters in the high-speed electronic section consist of 4-, 5-, 7-, and 11-stage counters. Two inputs are supplied to the counters; one for up-driving the storage section to the maximum storage count of 1540 bits, and the other for down-driving it to the minimum or zero count. The up-drive input consists of error pulses supplied by the error flip-flop in the receiver module. The down-drive input is supplied by a count-down one-shot circuit which, in turn, activates a 20/80 millisecond read-time one-shot circuit.

The upper and lower limits of the high-speed storage section are sensed in order to control the mechanical totalizer, the resynchronizing circuit, and the alarm system. An up-limit or overrun pulse is derived from the last stage of each ring counter. In operation, the ring counter outputs are connected to a four-input up-limit AND gate. When the 1540-bit up limit is reached, the AND function is fulfilled, and the AND gate develops an overrun pulse which sets the data resync flip-flop in the receiver module, activating the overrun alarm section. This action initiates pattern resynchronization in the receiver module.

The down-limit signal is derived from the first stage of each ring counter. In operation, the ring counter outputs are connected to a four-input down-limit AND gate. When all counters reach the zero or empty state, the AND function is fulfilled, and a down-limit clamp is routed to a count-down control NOR gate in the low-speed error readout section. The high-speed counters can be manually reset to zero state by means of the front panel CLEAR STORAGE switch. Such reset features may be required during initial setup or during system checkout.

B4.2.2 LOW-SPEED ERROR READOUT SECTION

The low-speed error readout section includes a 20-millisecond count-down one-shot, a 20/80-millisecond read-time one-shot, a four-input count-down NOR gate, and a mechanical totalizer. Inputs to the NOR gate consists of delayed clock pulses from the receiver module, down-limit pulses from the high-speed storage section, count-down pulses from the 20-millisecond one-shot, and read-time pulses from the 20/80-millisecond one-shot. When no error pulses are being received by the high-speed storage section and the ring counters reach the zero state, the 20-millisecond count-down one-shot is keyed off by a down-limit clamp from the counters by way of the control NOR gate. With the count-down one-shot thus inoperative, no pulses are applied to the read-time one-shot or to the mechanical totalizer.

Arrival of an error pulse from the receiver module advances the high-speed ring counter which, in turn, removes the down-limit clamp from the control NOR gate, thus allowing the next delayed clock pulse to set the count-down one-shot. Since the error pulse and delayed clock pulse are time displaced by one half clock cycle period, simultaneous application of up and down drive pulses to the high-speed counter is avoided. After the count-down one-shot returns to its stable state, the 20/80-millisecond one-shot is keyed on. Output from the count-down one-shot is routed to driver circuits which supply drive for the me-

chanical counter, external printer, and high-speed ring counters. The read-time one-shot provides sufficient time for the mechanical totalizer to release, or for the external printer to complete a cycle.

B4.2.3 OVERRUN ALARM SECTION

The overrun alarm section consists of a flip-flop, a driver circuit, a buzzer and lamp circuit, and an associated front panel switch. In operation, the flip-flop is set by an up-limit pulse from the high-speed counter. When thus set, the flip-flop turns on the driver stage, thereby activating both the buzzer and lamp alarm circuit. The alarm system is reset manually by means of a front panel DISABLE-ALARM-RESET switch. If use of the alarm is not required, the DISABLE-ALARM-RESET switch is set to DISABLE position. This position clamps the overrun flip-flop to reset.

B4.3 DETAILED CIRCUIT DESCRIPTION

The error counter module is divided into these three sections: a high-speed electronic storage section, a low-speed readout section, and an overrun alarm section. A detailed description of each section is presented in the following paragraphs.

B4.3.1 HIGH-SPEED ELECTRONIC STORAGE SECTION

The high-speed electronic storage section includes four ring counters which have a collective storage capacity of 1540 bits. Separately, the counters consist of 4-, 5-, 7-, and 11-stage counters as shown in Figures B6-2 through B6-4. Since the ring counters are identical except for the number of stages, only the 4-stage ring counter is described.

Refer to Figure B6-2. The 4-stage ring counter consists of transistor circuits Q12 through Q19. Each circuit contains a ring counter stage followed by an emitter-follower stage. Two inputs are applied to all four counter stages by way of separate diode gates. One input, called up-drive, consists of positive going error pulses from the receiver module. These pulses, applied at pin C, are inverted by up-count driver Q1, and the inverted output of Q1 is applied to diodes CR14 through CR17. The other input, called down-drive, is applied at pin M, to diodes CR19 through CR22. The down-drive input is supplied by a count-down one-shot circuit located on the counter control board of the low-speed readout section.

When power is initially applied to the Model 600F, all four ring counters are manually reset to zero by means of the front panel CLEAR STORAGE switch, S2. In the case of the 4-stage counter, this action turns off the first stage (Q12) and turns on the other three stages (Q14, Q16 and Q18). The off state of the first counter stage (Q12, Q13) primes diode gate (CR15, R63, C13) of the second counter stage. When an up-drive pulse arrives at pin C, the second counter stage is turned off; all other stages are turned on; and the third stage diode gate (CR16, R71, C15) is primed. Each succeeding up-drive pulse turns off the next counter stage and, in this manner, the counter is advanced.

After all four ring counters have reached the 1540-bit capacity, the last stage of each will be off, and an associated diode will be reverse-biased. This diode is CR18 in the 4-stage counter, CR8 in the 5-stage counter, CR9 in the 7-stage counter, and CR13 in the 11-stage counter. Together, the four diodes form the up-limit AND gate which develops a positive-going overrun pulse at pin J of Figure B6-2. This overrun pulse simultaneously sets the overrun flip-flop on the counter control board (Figure B6-5) and the resync flip-flop in the receiver module.

Down-drive operation is described by assuming that the second counter stage (Q14) is off and all other counter stages are on. This condition primes the diode gate (CR19, R59, C12) of the first stage (Q12). When a negative-going down-drive pulse appears at pin M, Q12 is turned off and Q14 is turned on. As a result, the count stored in the ring counters has been reduced by one. If the foregoing assumption is made for any other two counters stages, the effect will be the same. The succeeding stage prepares the preceeding stage to accept its count, and the down drive pulse completes the action.

After all four ring counters have reached the zero count condition, the first stage of each will be off, and an associated diode will be reverse-biased. This is diode CR2 in the 4-stage counter, CR1 in the 5-stage counter, CR2 in the 7-stage counter, and in the 11-stage counter. Together, the four diodes form the down-limit AND gate which develops a positive going pulse at pin F of Figure B6-2. This pulse is routed to the count-down control NOR gate located on the counter control board of the low-speed readout section.

B4.3.2 LOW-SPEED ERROR READOUT SECTION

Refer to Figure B6-5. The low-speed readout section includes a 20-millisecond count-down one-shot circuit (Q3-Q4), a 20/80-millisecond read-time one-shot circuit (Q7-Q8), a count-down control NOR gate (Q2),

and a front panel mechanical totalizer (M1). The three major functions performed by the low-speed error readout section are as follows: it provides a 20-millisecond drive pulse through a power amplifier to the mechanical totalizer; it provides the proper internal timing between drive pulses; and it generates a short trigger pulse for driving the count down line of the high-speed buffer storage section.

Count-down NOR gate Q2 is controlled by four inputs as follows: delayed clock pulses at pin L from the receiver module during permissible count-down times, down-limit pulses at pin M from the high-speed buffer storage section, count-down pulses from Q3 of the count-down one-shot circuit, and read-time pulses from Q7 of the read-time one-shot circuit. A fifth control input at pin N, providing for an external printer inhibit input, is not used in the Model 600F.

When the ring counters in the high-speed buffer storage section are in the reset state, the down-limit gate input at pin M is positive, and Q2 is held on. If, however, errors have been accumulating in the buffer storage section, the down-limit gate input is zero, and negative-going delayed clock pulses at pin L momentarily turn off Q2. The resultant positive going output from Q2 collector turns on Q4, thereby causing C2 to discharge through R11, turning off Q3 in a standard one-shot fashion. The pulse duration of Q3-Q4 is a nominal 20 milliseconds. As Q3 turns off, its positive-going collector signal causes Q2 to turn on, holding the gate closed.

As Q4 is triggered on, its collector goes from a positive potential to ground. This action discharges C1 through R15, causing count-down inverter Q5 to turn off and count-down driver Q6 to turn on. The resultant collector output of Q6 is routed through pin J to the count-down line of the high-speed buffer storage section.

At the end of the 20-millisecond timing interval, the count-down one-shot circuit returns to its normal state. Simultaneously, the collector of Q3 goes to zero and triggers read-time one-shot Q7-Q8. The positive-going output at Q7 then assumes control of Q2 by holding the gate closed. Q7-Q8 has two possible cycle times as determined by rear panel connections through pin K. Pin K is wired to the RATE terminal, 1, on the rear panel terminal board, TB1, of the Model 600F. When pin K is grounded, the cycle time is a nominal 20 milliseconds. The summation of the two one-shot times is approximately 40 milliseconds, about 25 pulses-per-second for the mechanical totalizer.

When the Model 600F is used with an external printer, the RATE terminal is ungrounded. This action allows C4 to charge to a high potential, thus lengthening the time of the read-time one-shot to approximately 80 milliseconds. The summation of the two one-shot times is then approximately 100 milliseconds, which is about 10 pulses-per-second for the external printer counter.

The charges on one-shot timing capacitors C2 and C4 are limited by voltage dividers R19-R20, and R26-R27 respectively. This feature prevents fluctuations on the +12 volt power supply line from falsely triggering the one-shots. Diodes CR2 and CR4, which permit charging of the timing capacitors, decouple the capacitors whenever the +12 volt line drops below a certain level.

Counter driver stage Q14 is a power transistor which provides current switching for the front panel mechanical totalizer. Drive current for the totalizer is obtained from the +15 volt section of the power supply module. In operation, a 20-millisecond pulse from the count-down one-shot is coupled through the emitter-follower, Q13, to the base of Q14. When Q13 is turned on, it saturates and permits base drive current for Q14 to be developed through R33. The collector saturation voltage of Q13 is the sum of the base-emitter drop of Q14 and the collector-emitter drop of Q13, about 0.8 volt.

Transistor stage Q9 is an auxiliary driver which provides a count output for the external printer. Q9 is normally off because Q13 is normally off. As a result, the collector of Q13 is at +15 volts, and the ratio of R32 to R34 maintains the base of Q9 at a slightly positive potential with respect to its emitter. When Q13 is turned on, its collector voltage falls to approximately 1 volt. Turn-on drive current for Q9 is then supplied through R34, since the hold-off current through R32 has now disappeared.

B4.3.3 OVERRUN ALARM SECTION

Refer to Figure B6-5. The overrun alarm section includes a flip-flop, Q10-Q11, and an alarm driver, Q12. The flip-flop is triggered by an overrun pulse from the high-speed buffer storage section when its capacity is exceeded: at that time the flip-flop activates the alarm driver which controls the buzzer, DS1, and front panel ALARM lamp, DS2. Prior to arrival of an overrun pulse, the flip-flop Q10-Q11 is in the reset state, with Q10 on and Q11 off. Under this condition, current flows through Q10 and diode CR7 to hold Q12 off. When an overrun pulse

arrives at pin F from the up-limit gate, the flip-flop is set, and Q12 is turned on. This action connects ALARM lamp DS2 and buzzer DS1 across the power supply. DS2 is connected directly to the negative rectifiers in the power supply module (see Figure 6-16) and receives unfiltered current. DS1 is connected through a diode and resistor to one side of the power transformer secondary in the power supply module. This latter connection provides a 60-hertz pulsating direct current to DS1.

The overrun alarm flip-flop is manually reset by means of the front panel ALARM-DISABLE-RESET switch, S1 (see Figure B6-6). The RESET position of S1 momentarily grounds the collector of Q10, thereby restoring the flip-flop to the off, or reset, state. The DISABLE position permits the ALARM lamp and buzzer circuit to be permanently disconnected. The DISABLE position connects a ground to the Q10 collector and thus prevents the flip-flop from being triggered.

SECTION B5

MAINTENANCE

B5.1 GENERAL

This section contains information concerning maintenance of the Model 600 Error Counter Module, and parts lists for items that may require replacement due to wear, deterioration, mechanical breakage or burnout. Both preventive maintenance, which includes a schedule of general inspection procedures and cleaning, and corrective maintenance, which includes a table of troubleshooting procedures, are presented. Although some preventive maintenance will normally be performed by the operator, all corrective maintenance should be performed by a qualified technician who should have a thorough understanding of the Model 600 Error Counter Module circuitry.

B5.2 PREVENTIVE MAINTENANCE

B5.2.1 INSPECTION

A general component inspection procedure is shown in Table B5-1. Regularly scheduled inspection of the equipment will assist the operating personnel in detecting potential troubles and correcting them before failures occur. A semi-annual inspection is sufficient. More frequent inspection may be necessary, however, if the equipment is operated in a poor environment or is otherwise harshly treated.

B5.2.2 CLEANING

The equipment should be kept dry and free from dirt, grease, and oil. Any regularly scheduled cleaning routine should include removal of dust from the equipment interior and exterior. Avoid using sharp cleaning tools which can scratch surfaces or damage printed circuit boards. Instead, use a soft brush or rag to prevent dirt build-up and possible short circuits.

B5.3 CORRECTIVE MAINTENANCE

Corrective maintenance procedures generally involve visual observation of operating conditions to localize the cause of malfunction to a specific area. The troubleshooting chart contained in Table B5-2 will

Table B5-1

GENERAL INSPECTION PROCEDURES

Component	Condition	Cause	Correction
Resistors	Discolored, swollen, or cracked	Overheated	Correct overload condition and replace defective resistors.
Capacitors	Leakage, bulging, split case, or broken end seals	Physical damage or dielectric breakdown	Replace defective capacitor.
Connectors and jacks	Bent pins, charred insulation, marred threads moisture, dirt, or grease	Improper handling	Straighten pins, clean or replace part.
Switches and controls	Broken, worn, bent, or dirty	Rough handling, normal wear	Clean, straighten, or replace.
Indicator Lamps	Broken or burnt out	Rough handling, excessive current	If broken, replace; if burnt out, check circuit for possible cause. Correct cause of burnt-out lamp and replace lamp.
Wiring and Cables	Cut or frayed insulation, broken wires or connections	Improper handling	Repair or replace.
Solder connections	Loose or corroded connections, cold solder joints	Improper soldering	Clean and resolder.

Table B5-2

MODEL 600 ERROR COUNTER MODULE TROUBLESHOOTING CHART

Symptom	Probable Cause	Remedy
Error totalizer does not count during error test operation	1. If error lamp lights when error switch is in LAMP position, the mechanical totalizer is defective	1. Replace defective mechanical totalizer
	2. No error pulses from receiver module	2. Troubleshoot error detection circuits on PC board NO39079 of receiver module
	3. Buffer storage ring counters do not advance	3. Troubleshoot ring counter reset circuits on PC boards NO351, NO352, and NO354
	4. Defective error read-out control circuits	4. Troubleshoot error read-out circuits on PC board NO353
Overrun of error storage occurs early (see steps g and h, paragraph B5.4)	1. One or more of the buffer storage ring counters is defective	1. Troubleshoot ring counter circuits on PC board NO351, NO352, and NO354

provide the service technician with a systematic procedure for locating and repairing equipment troubles. The only test equipment required is an electronic frequency counter (ATEC 6C46 or equivalent).

Table B5-2 uses the familiar "symptom, probable cuase, and remedy" approach. If spare printed circuit boards are available, troubles can be quickly isolated by substituting boards. Schematic diagrams contained in Section B6 should be used during troubleshooting operations.

B5.4 PERFORMANCE TEST

To test the performance of the Model 600 Error Counter Module in module position A4 of Model 600F Data Transmission Test Set, proceed as follows:

a. Perform initial setup of Model 600F as given in steps a through e, paragraph 5.4.5.1 of instruction manual for Model 600F.

b. Set POWER ON switch to ON position.

c. On error counter module depress reset lever on mechanical totalizer; depress CLEAR STORAGE pushbutton switch; set COUNT-ERROR-LAMP switch to COUNT position; and set DISABLE-ALARM-RESET switch to ALARM position.

d. Set pattern generator TX CLK switch to SCT position and observe that error counter counts or indicates errors and that an overrun of error storage occurs as indicated by visual and audible alarms. The SYNC ALARM lamp on the receiver module should light when overrun condition occurs.

e. Set pattern generator TX CLK switch to SCTE position.

f. On error counter module reset mechanical totalizer; depress CLEAR STORAGE pushbutton switch; and operate DISABLE-ALARM-RESET switch momentarily to RESET position.

g. Connect electronic frequency counter to the ERROR PULSE BNC connector on the receiver module; and set

control on frequency counter to MANUAL mode.

h. Set pattern generator TX CLK switch to SCT position, and observe that when error counter overrun occurs, frequency counter reading is approximately equal to sum of mechanical totalizer reading and 1540 bit storage capacity of ring counters.

B5.5 PARTS LISTS

Parts (except hardware) contained in the Model 600 Error Counter Module are listed in Tables B5-3 through B5-7. Items in each table are listed according to assembly figure number, part designator, part description, manufacturer's part number, manufacturer, and quantity. A list of manufacturers is provided in Table B5-8.

Table B5-3

MODEL 600 ERROR COUNTER MODULE A4

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-11	A4	Error Counter Assembly	DO861	FEC	1
B6-11	A4A1	Assembly, 4- and 5-stage ring counter	DO914	FEC	1
B6-11	A4A2	Assembly, 7-stage ring counter	DO913	FEC	1
B6-11	A4A3	Assembly, counter control	DO910	FEC	1
B6-11	A4A4	Assembly, 11-stage ring counter	DO912	FEC	1
B6-11	A4DS1	Buzzer	1001-89	Price Elec.	1
B6-11	A4DS2	Lamp	327	G.E.	1
B6-11	A4DS3	Lamp	330	G.E.	1
B6-11	A4J1 thru J4	Connector	250-15-30-160	Cinch-Jones	4
B6-11	A4M1	Counter, 4-digit, mechanical	TCeZ4E.25	Landis and Gyr Importers for SODECO	1

Table B5-3

MODEL 600 ERROR COUNTER MODULE A4 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-11	A4P1	Connector	26-149-24	Amphenol-Borg	1
B6-11	A4R1	Resistor, fixed carbon comp., 120 ohms, 1/4 w, 10%	RC07GF121K	Mil. Std.	1
B6-11	A4S1	Switch, toggle, SPDT, spring return	MST105H	ALCO	1
B6-11	A4S2	Switch, pushbutton	953	Switchcraft	1
B6-11	A4S3	Switch, toggle, SPDT	MST115D	ALCO	1
B6-11	A4X1, X2	Lamp Assembly	162-8430-931	Dialight	2

Table B5-4

4- AND 5-STAGE RING COUNTERS PC BOARD A4A1

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-7	A4A1E1	Printed Circuit Board	NO351	FEC	1
B6-7	C1 thru C18	Capacitor, fixed, ceramic dielectric, 220 pf, 500 v	831Z5F221K	Erie	18
B6-7	CR1 thru CR22	Diode	1N4009	G.E.	22
B6-7	Q1, Q2	Transistor, NPN	2N3605	G.E.	2
B6-7	Q3	Transistor, NPN	2N3394	G.E.	1
B6-7	Q4	Same as Q1			1
B6-7	Q5	Same as Q3			1
B6-7	Q6	Same as Q1			1
B6-7	Q7	Same as Q3			1
B6-7	Q8	Same as Q2			1
B6-7	Q9	Same as Q3			1

Table B5-4

4- AND 5-STAGE RING COUNTERS PC BOARD A4A1 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-7	Q10	Same as Q2			1
B6-7	Q11	Same as Q3			1
B6-7	Q12	Same as Q2			1
B6-7	Q13	Same as Q3			1
B6-7	Q14	Same as Q2			1
B6-7	Q15	Same as Q3			1
B6-7	Q16	Same as Q2			1
B6-7	Q17	Same as Q3			1
B6-7	Q18	Same as Q2			1
B6-7	Q19	Same as Q3			1
B6-7	R1, R2	Resistor, fixed, carbon comp., 4700 ohms, 1/4w; 10%	RC07GF472K	Mil. Std.	2

Table B5-4

4- AND 5-STAGE RING COUNTERS PC BOARD A4A1 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-7	R3	Resistor, fixed, carbon comp., 12,000 ohms, 1/4 w, 10%	RC07GF123K	Mil. Std.	1
B6-7	R4, R5, R6	Resistor, fixed, carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Mil. Std.	3
B6-7	R7	Resistor, fixed, carbon comp., 120 ohms, 1/4 w, 10%	RC07GF121K	Mil. Std.	1
B6-7	R8	Same as R2			1
B6-7	R9	Resistor, fixed, carbon comp., 22,000 ohms, 1/4 w, 10%	RC07GF223K	Mil. Std.	1
B6-7	R10 thru R13	Resistor, fixed, carbon comp., 6800 ohms, 1/4 w, 10%	RC07GF682K	Mil. Std.	4
B6-7	R14	Same as R9			1
B6-7	R15	Same as R6			1
B6-7	R16	Same as R7			1

Table B5-4

4- AND 5-STAGE RING COUNTERS PC BOARD A4A1 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-7	R17	Same as R2			1
B6-7	R18	Same as R9			1
B6-7	R19 thru R22	Same as R13			4
B6-7	R23	Same as R9			1
B6-7	R24	Same as R6			1
B6-7	R25	Same as R7			1
B6-7	R26	Same as R2			1
B6-7	R27	Same as R9			1
B6-7	R28 thru R31	Same as R13			4
B6-7	R32	Same as R9			1
B6-7	R33	Same as R6			1

Table B5-4

4- AND 5-STAGE RING COUNTERS PC BOARD A4A1 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-7	R34	Same as R7			1
B6-7	R35	Same as R2			1
B6-7	R36	Same as R9			1
B6-7	R37 thru R40	Same as R13			4
B6-7	R41	Same as R9			1
B6-7	R42	Same as R6			1
B6-7	R43	Same as R7			1
B6-7	R44	Same as R2			1
B6-7	R45	Same as R9			1
B6-7	R46 thru R49	Same as R13			4
B6-7	R50	Same as R9			1

Table B5-4

4- AND 5-STAGE RING COUNTERS PC BOARD A4A1 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-7	R51	Same as R2			1
B6-7	R52	Same as R6			1
B6-7	R53	Same as R7			1
B6-7	R54	Same as R2			1
B6-7	R55	Same as R9			1
B6-7	R56, R57, R58	Same as R13			3
B6-7	R59	Same as R9			1
B6-7	R60	Same as R6			1
B6-7	R61	Same as R7			1
B6-7	R62	Same as R2			1
B6-7	R64, R65, R66	Same as R13			3

Table B5-4

4- AND 5-STAGE RING COUNTERS PC BOARD A4A1 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-7	R67	Same as R9			1
B6-7	R68	Same as R6			1
B6-7	R69	Same as R7			1
B6-7	R70	Same as R2			1
B6-7	R71	Same as R9			1
B6-7	R72, R73, R74	Same as R13			3
B6-7	R75	Same as R9			1
B6-7	R76	Same as R6			1
B6-7	R77	Same as R7			1
B6-7	R78	Same as R2			1
B6-7	R79	Same as R9			1

Table B5-4

4- AND 5-STAGE RING COUNTERS PC BOARD A4A1 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-7	R80, R81, R82	Same as R13			3
B6-7	R83	Same as R9			1

Table B5-5

7-STAGE RING COUNTER PC BOARD A4A2

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-8	A4A2E1	Printed Circuit Board	NO352	FEC	1
B6-8	C1 thru C14	Capacitor, fixed, ceramic dielectric, 220 pf, 500 v	831Z5F221K	Erie	14
B6-8	CR1 thru CR16	Diode	1N4009	G.E.	16
B6-8	Q1	Transistor, NPN	2N3605	G.E.	1
B6-8	Q2	Transistor, NPN	2N3394	G.E.	1
B6-8	Q3	Same as Q1			1
B6-8	Q4	Same as Q2			1
B6-8	Q5	Same as Q1			1
B6-8	Q6	Same as Q2			1
B6-8	Q7	Same as Q1			1
B6-8	Q8	Same as Q2			1

Table B5-5

7-STAGE RING COUNTER PC BOARD A4A2 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-8	Q9	Same as Q1			1
B6-8	Q10	Same as Q2			1
B6-8	Q11	Same as Q1			1
B6-8	Q12	Same as Q2			1
B6-8	Q13	Same as Q1			1
B6-8	Q14	Same as Q2			1
B6-8	R1	Resistor, fixed, carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Mil. Std.	1
B6-8	R2, R3	Resistor, fixed, carbon comp., 120 ohms, 1/4 w, 10%	RC07GF121K	Mil. Std.	2
B6-8	R4	Resistor, fixed, carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Mil. Std.	1
B6-8	R5	Same as R1			1

Table B5-5

7-STAGE RING COUNTER PC BOARD A4A2 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-8	R6, R7	Same as R3			2
B6-8	R8	Same as R4			1
B6-8	R9	Same as R1			1
B6-8	R10, R11	Same as R3			2
B6-8	R12	Same as R4			1
B6-8	R13	Same as R1			1
B6-8	R14, R15	Same as R3			2
B6-8	R16	Same as R4			1
B6-8	R17	Same as R1			1
B6-8	R18, R19	Same as R3			2
B6-8	R20	Same as R4			1
B6-8	R21	Same as R1			1

Table B5-5

7-STAGE RING COUNTER PC BOARD A4A2 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-8	R22, R23	Same as R3			2
B6-8	R24	Same as R4			1
B6-8	R25	Same as R1			1
B6-8	R26, R27	Same as R3			2
B6-8	R28	Same as R4			1
B6-8	R29	Resistor, fixed, carbon comp., 22,000 ohms, 1/4 w, 10%	RC07GF223K	Mil. Std.	1
B6-8	R30 thru R35	Resistor, fixed, carbon comp., 6800 ohms, 1/4 w, 10%	RC07GF682K	Mil. Std.	6
B6-8	R36, R37	Same as R29			2
B6-8	R38 thru R43	Same as R35			6
B6-8	R44, R45	Same as R29			2

Table B5-5

7-STAGE RING COUNTER PC BOARD A4A2 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-8	R46 thru R51	Same as R35			6
B6-8	R52, R53	Same as R29			2
B6-8	R54 thru R59	Same as R35			6
B6-8	R60, R61	Same as R29			2
B6-8	R62 thru R67	Same as R35			6
B6-8	R68, R69	Same as R29			2
B6-8	R70 thru R75	Same as R35			6
B6-8	R76, R77	Same as R29			2
B6-8	R78 thru R83	Same as R35			6
B6-8	R84	Same as R29			1

Table B5-6

COUNTER CONTROL PC BOARD A4A3

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-10	A4A3E1	Printed Circuit Board	NO353	FEC	1
B6-10	C1	Capacitor, fixed, ceramic dielectric, 820 pf, 500 v	831Z5F821K	Erie	1
B6-10	C2	Capacitor, fixed, tantalum electrolytic, 4.7 μf, 35 vdc	150D475X90-35B2	Sprague	1
B6-10	C3	Capacitor, fixed, ceramic dielectric 0.01 μf, 25 v	5835Y5U103Z	Erie	1
B6-10	C4	Capacitor, fixed, tantalum electrolytic, 6.8 μf, 35 vdc	150D685X90-35B2	Sprague	1
B6-10	C5	Capacitor, fixed, ceramic dielectric, 220 pf, 500 v	831Z5F221K	Erie	1
B6-10	CR1 thru CR5	Diode	1N483B	Texas Instr.	5
B6-10	CR6	Diode	1N4009	G.E.	1
B6-10	CR7	Same as CR5			1

Table B5-6

COUNTER CONTROL PC BOARD A4A3 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-10	Q1	Transistor, NPN	2N3394	G. E.	1
B6-10	Q2, Q3	Transistor, NPN	2N3605	G. E.	2
B6-10	Q4	Same as Q1			1
B6-10	Q5, Q6	Same as Q3			2
B6-10	Q7, Q8	Same as Q1			2
B6-10	Q9	Transistor, PNP	2N404	G. E.	1
B6-10	Q10, Q11	Same as Q3			2
B6-10	Q12	Transistor, PNP	2N526	G. E.	2
B6-10	Q13	Same as Q1			1
B6-10	Q14	Transistor, NPN	40318	RCA	1
B6-10	R1, R2	Resistor, fixed, carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Mil. Std.	2

Table B5-6

COUNTER CONTROL PC BOARD A4A3 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-10	R3	Resistor, fixed, carbon comp., 12,000 ohms, 1/4 w, 10%	RC07GF123K	Mil. Std.	1
B6-10	R4 thru R7	Same as R2			4
B6-10	R8	Resistor, fixed, carbon comp., 47,000 ohms, 1/4 w, 10%	RC07GF473K	Mil. Std.	1
B6-10	R9, R10	Same as R2			2
B6-10	R11	Resistor, fixed, carbon comp., 15,000 ohms, 1/4 w, 10%	RC07GF153K	Mil. Std.	1
B6-10	R12	Resistor, fixed, carbon comp., 1200 ohms, 1/4 w, 10%	RC07GF122K	Mil. Std.	1
B6-10	R13	Same as R2			1
B6-10	R14	Same as R8			1
B6-10	R15	Resistor, fixed, carbon comp., 22,000 ohms, 1/4 w, 10%	RC07GF223K	Mil. Std.	1

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Table B5-6

COUNTER CONTROL PC BOARD A4A3 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-10	R16	Same as R2			1
B6-10	R17, R18, R19	Resistor, fixed, carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Mil. Std.	3
B6-10	R20	Same as R12			1
B6-10	R21	Same as R2			1
B6-10	R22	Resistor, fixed, carbon comp., 33,000 ohms, 1/4 w, 10%	RC07GF333K	Mil. Std.	1
B6-10	R23	Same as R19			1
B6-10	R24	Same as R2			1
B6-10	R25	Same as R15			1
B6-10	R26	Same as R19			1
B6-10	R27	Resistor, fixed, carbon comp., 2700 ohms, 1/4 w, 10%	RC07GF272K	Mil. Std.	1

Table B5-6

COUNTER CONTROL PC BOARD A4A3 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-10	R28	Resistor, fixed, carbon comp., 470 ohms, 1/4 w, 10%	RC07GF471K	Mil. Std.	1
B6-10	R29	Same as R2			1
B6-10	R30, R31	Same as R8			2
B6-10	R32	Same as R19			1
B6-10	R33	Resistor, fixed, carbon comp., 470 ohms, 1/2 w, 10%	RC20GF471K	Mil. Std.	1
B6-10	R34	Resistor, fixed, carbon comp., 3300 ohms, 1/4 w, 10%	RC07GF332K	Mil. Std.	1
B6-10	R35	Resistor, fixed, carbon comp.,	RC07GF470K	Mil. Std.	1
B6-10	R36	Same as R2			1
B6-10	R37	Same as R33			1
B6-10	R38, R39	Same as R2			2

Table B5-6

COUNTER CONTROL PC BOARD A4A3 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-10	R40	Same as R8			1
B6-10	R41, R42	Same as R12			2
B6-10	R43	Same as R2			1
B6-10	R44	Same as R8			1
B6-10	R45	Same as R19			1
B6-10	R46	Same as R2			1

Table B5-7

11-STAGE RING COUNTER PC BOARD A4A4

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-9	A4A4E1	Printed Circuit Board	NO354	FEC	1
B6-9	C1 thru C22	Capacitor, fixed, ceramic dielectric, 220 pf, 500 v	831Z5F221K	Erie	22
B6-9	CR1 thru CR24	Diode	1N4009	G.E.	24
B6-9	Q1	Transistor, NPN	2N3394	G.E.	1
B6-9	Q2	Transistor, NPN	2N3605	G.E.	1
B6-9	Q3	Same as Q1			1
B6-9	Q4	Same as Q2			1
B6-9	Q5	Same as Q1			1
B6-9	Q6	Same as Q2			1
B6-9	Q7	Same as Q1			1
B6-9	Q8	Same as Q2			1

Table B5-7

11-STAGE RING COUNTER PC BOARD A4A4 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-9	Q9	Same as Q1			1
B6-9	Q10	Same as Q2			1
B6-9	Q11	Same as Q1			1
B6-9	Q12	Same as Q2			1
B6-9	Q13	Same as Q1			1
B6-9	Q14	Same as Q2			1
B6-9	Q15	Same as Q1			1
B6-9	Q16	Same as Q2			1
B6-9	Q17	Same as Q1			1
B6-9	Q18	Same as Q2			1
B6-9	Q19	Same as Q1			1
B6-9	Q20	Same as Q2			1

Table B5-7

11-STAGE RING COUNTER PC BOARD A4A4 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-9	Q21	Same as Q1			1
B6-9	Q22	Same as Q2			1
B6-9	R1	Resistor, fixed, carbon comp., 2200 ohms, 1/4 w, 10%	RC07GF222K	Mil. Std.	1
B6-9	R2, R3	Resistor, fixed, carbon comp., 120 ohms, 1/4 w, 10%	RC07GF121K	Mil. Std.	2
B6-9	R4	Resistor, fixed carbon comp., 4700 ohms, 1/4 w, 10%	RC07GF472K	Mil. Std.	1
B6-9	R5	Same as R1			1
B6-9	R6, R7	Same as R3			2
B6-9	R8	Same as R4			1
B6-9	R9	Same as R1			1
B6-9	R10, R11	Same as R3			2

Table B5-7

11-STAGE RING COUNTER PC BOARD A4A4 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-9	R12	Same as R4			1
B6-9	R13	Same as R1			1
B6-9	R14, R15	Same as R3			2
B6-9	R16	Same as R4			1
B6-9	R17	Same as R1			1
B6-9	R18, R19	Same as R3			2
B6-9	R20	Same as R4			1
B6-9	R21	Same as R1			1
B6-9	R22, R23	Same as R3			2
B6-9	R24	Same as R4			1
B6-9	R25	Same as R1			1
B6-9	R26, R27	Same as R3			2

Table B5-7

11-STAGE RING COUNTER PC BOARD A4A4 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-9	R28	Same as R4			1
B6-9	R29	Same as R1			1
B6-9	R30, R31	Same as R3			2
B6-9	R32	Same as R4			1
B6-9	R33	Same as R1			1
B6-9	R34, R35	Same as R3			2
B6-9	R36	Same as R4			1
B6-9	R37	Same as R1			1
B6-9	R38, R39	Same as R3			2
B6-9	R40	Same as R4			1
B6-9	R41	Same as R1			1
B6-9	R42, R43	Same as R3			2

Table B5-7

11-STAGE RING COUNTER PC BOARD A4A4 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-9	R44	Same as R4			1
B6-9	R45	Resistor, fixed, carbon comp., 22,000 ohms, 1/4 w, 10%	RC07GF223K	Mil. Std.	1
B6-9	R46 thru R55	Resistor, fixed, carbon comp., 6800 ohms, 1/4 w, 10%	RC07GF682K	Mil. Std.	10
B6-9	R56, R57	Same as R45			2
B6-9	R58 thru R67	Same as R55			10
B6-9	R68, R69	Same as R45			2
B6-9	R70 thru R79	Same as R55			10
B6-9	R80, R81	Same as R45			2
B6-9	R82 thru R91	Same as R55			10

Table B5-7

11-STAGE RING COUNTER PC BOARD A4A4 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-9	R92, R93	Same as R45			2
B6-9	R94 thru R103	Same as R55			10
B6-9	R104, R105	Same as R45			2
B6-9	R106 thru R115	Same as R55			10
B6-9	R116, R117	Same as R45			2
B6-9	R118 thru R127	Same as R55			10
B6-9	R128, R129	Same as R45			2
B6-9	R130 thru R139	Same as R55			10
B6-9	R140, R141	Same as R45			2
B6-9	R142 thru R151	Same as R55			10

Table B5-7

11-STAGE RING COUNTER PC BOARD A4A4 (Cont)

Fig. No.	Ref. Desig.	Description	Mfr. Part No.	Mfr.	Qty.
B6-9	R152, R153	Same as R45			2
B6-9	R154 thru R163	Same as R55			10
B6-9	R164, R165	Same as R45			2
B6-9	R166 thru R175	Same as R55			10
B6-9	R176	Same as R45			1

Table B5-8

LIST OF MANUFACTURERS

Manufacturer	Manufacturer's Address
ALCO	ALCO Electronics Products, Incorporated 3 Walcott Avenue Lawrence, Massachusetts 01843
Amphenol-Borg	The Bunker-Ramo Corporation Amphenol Connector Division 2801 South 25th Avenue Broadview, Illinois 60153
Cinch-Jones	Cinch Manufacturing Company and Howard B. Jones Division 1026 South Homan Avenue Chicago, Illinois 60624
Dialight	Dialight Corporation 60 Stewart Avenue Brooklyn, New York 11237
Erie	Erie Technological Products Incorporated 644 West 12th Street Erie, Pennsylvania 16512
FEC	Frederick Electric Corporation P.O. Box 502 Frederick, Maryland 21701
G.E.	General Electric Company Semiconductor Products Department Electronics Park Syracuse, New York 13201
Landis and Gyr	Landis and Gyr Incorporated 45 West 45th Street New York, New York 10036

Table B5-8

LIST OF MANUFACTURERS (Cont)

Manufacturer	Manufacturer's Address
Mil. Std.	Military Standard
Price Elec.	Price Electric Company Division of North American Phillips Corporation 5560 Church Street Frederick, Maryland 21701
RCA	RCA Corporation Solid State Division Route 202 Somerville, New Jersey 08876
Sprague	Sprague Electric Company North Adams, Massachusetts 01247
Switchcraft	Switchcraft Incorporated 5555 North Elston Avenue Chicago, Illinois 60630
Texas Instr.	Texas Instrument, Incorporated Semiconductor Components Division 13500 North Central Expressway Dallas, Texas 75231

SECTION B6

DRAWINGS

This section includes schematic and assembly diagrams of printed circuit boards contained in the Model 600 Error Counter Module, wiring and assembly diagrams of the module, and a functional block diagram to show the relationship of circuits in the module.

The functional block diagram is shown in Figure B6-1. Lists of schematic, wiring, and assembly diagrams are provided in Tables B6-1 and B6-2.

Table B6-1

SCHEMATIC AND WIRING DIAGRAMS

Table B6-2

ASSEMBLY DIAGRAMS

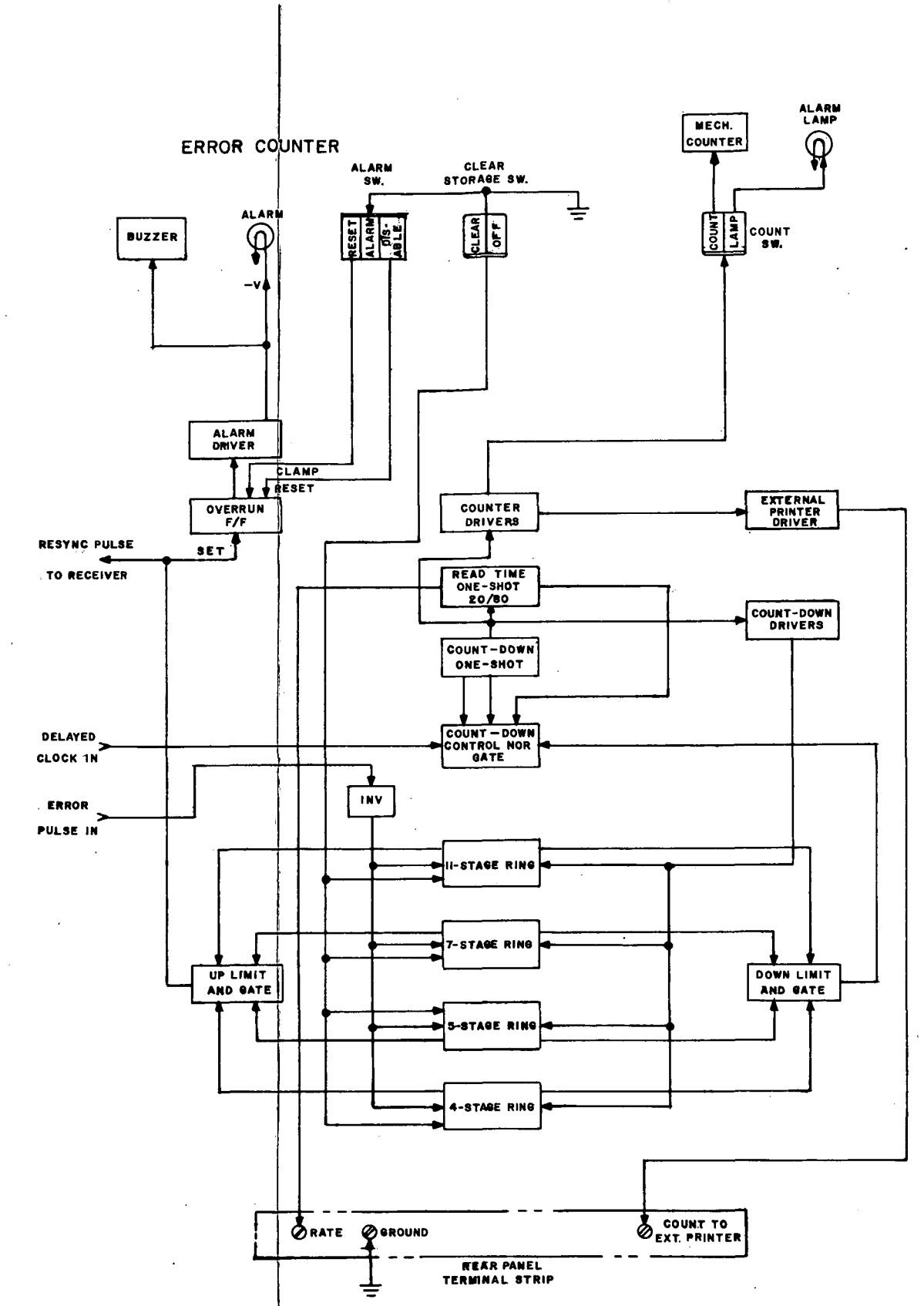
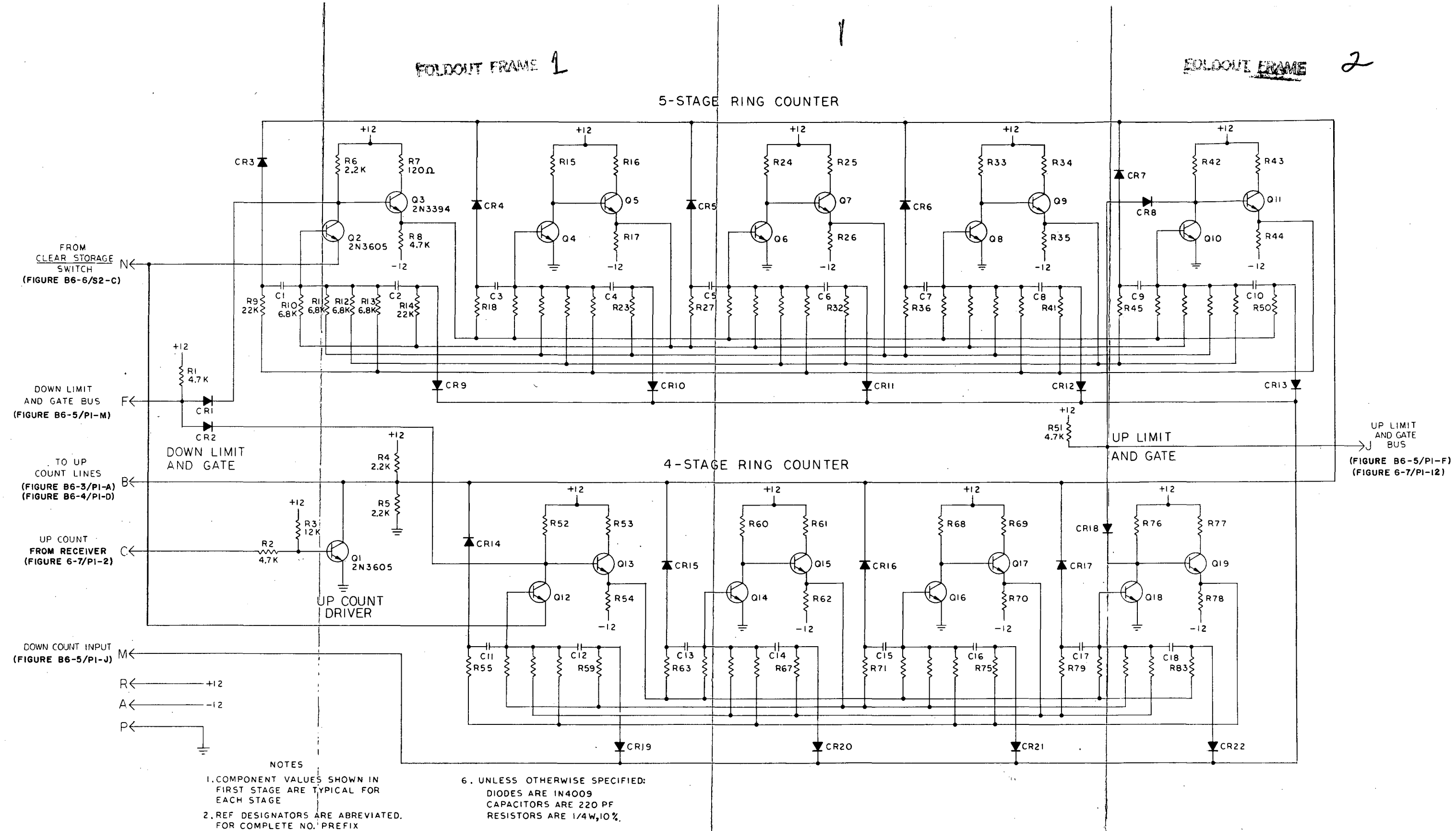


Figure B6-1. Model 600 Error Counter Module Functional Block Diagram

FOLDOUT FRAME 1

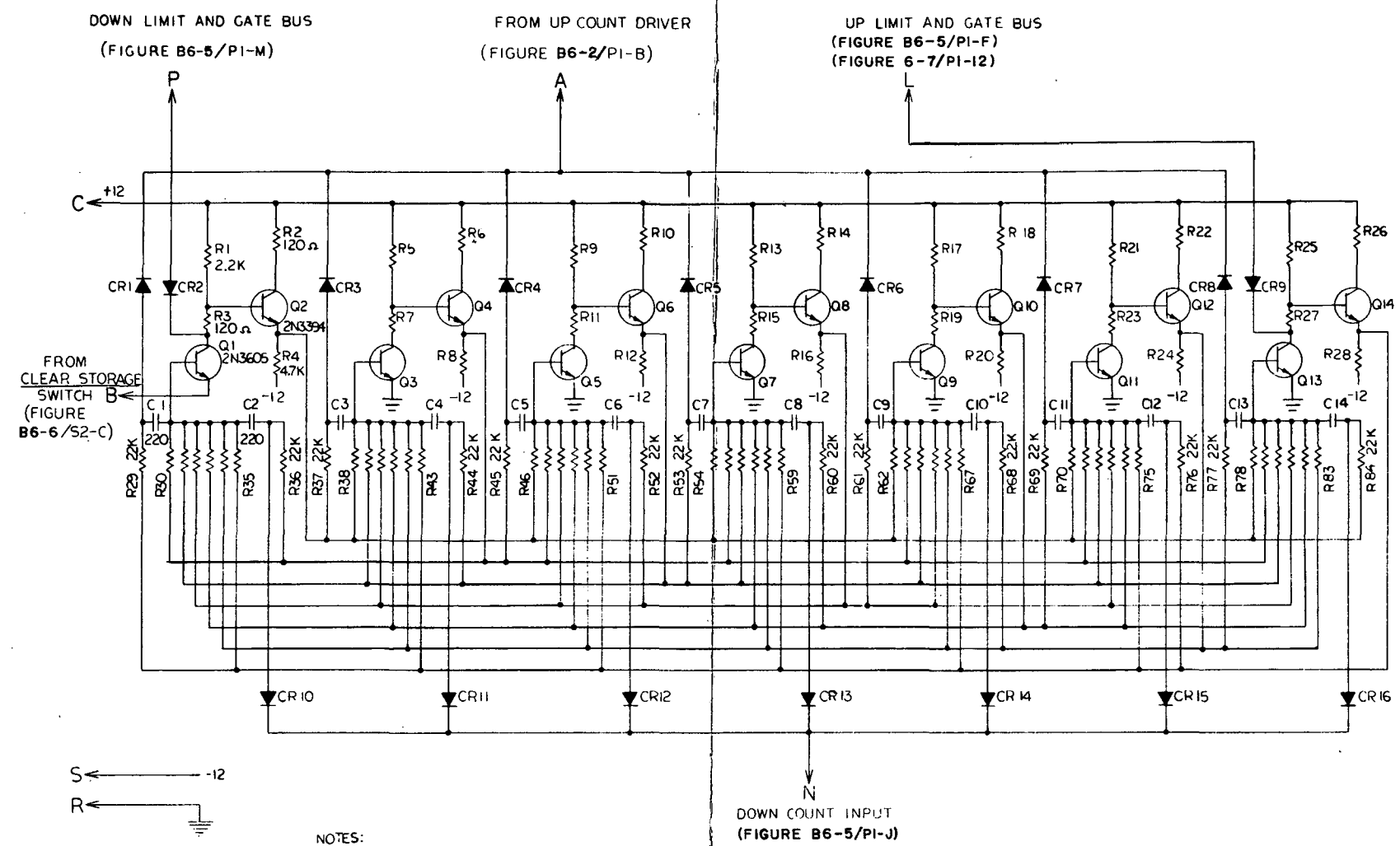
FOLDOUT FRAME 2



NOTES

1. COMPONENT VALUES SHOWN IN FIRST STAGE ARE TYPICAL FOR EACH STAGE
2. REF DESIGNATORS ARE ABREVIATED. FOR COMPLETE NO. PREFIX DESIGNATOR WITH ASS'Y NO. A4A1.
3. PLUG DESIGNATOR IS P1.
4. P. C. BOARD REF NO351.
5. P. C. BOARD ASS'Y REF D0914.
6. UNLESS OTHERWISE SPECIFIED:
   DIODES ARE IN4009
   CAPACITORS ARE 220 PF
   RESISTORS ARE 1/4W,10%.

Figure B6-2. 4- and 5-Stage Ring Counters Schematic Diagram



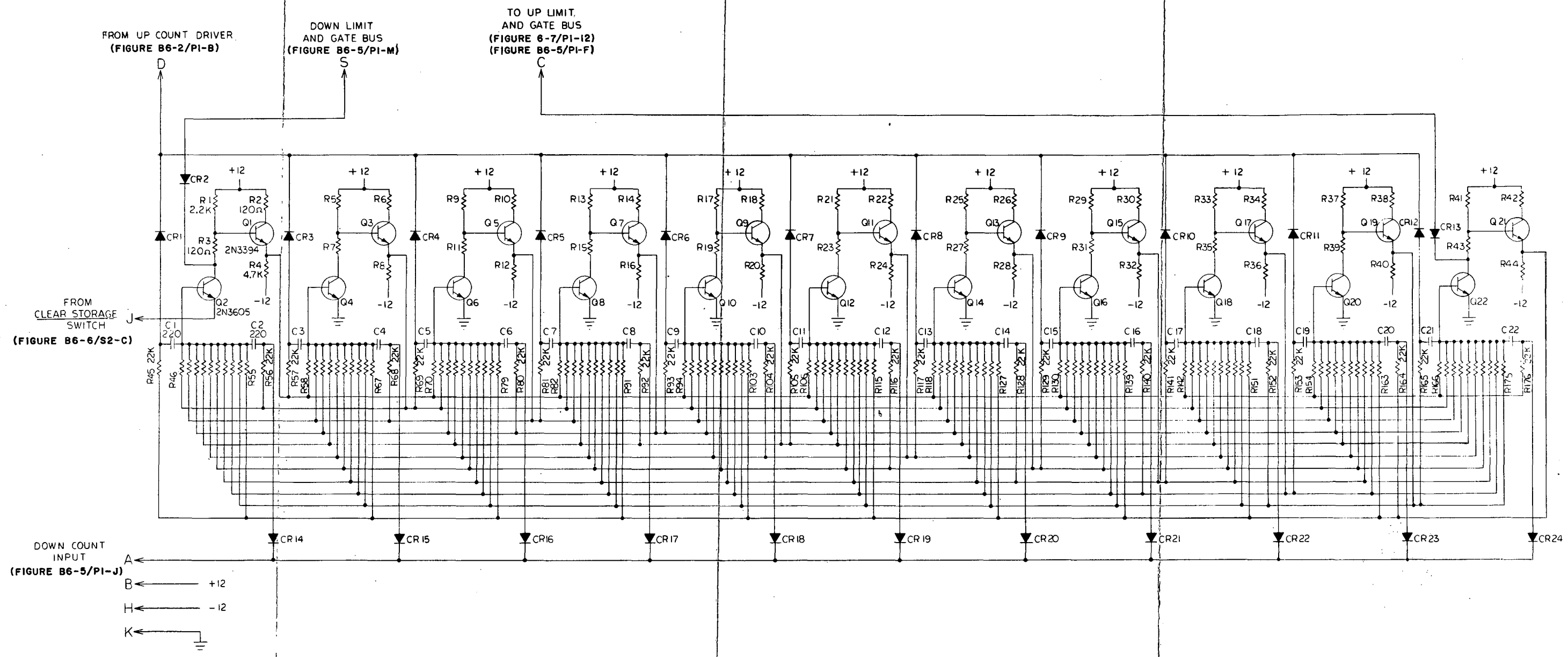
NOTES:

1. COMPONENT VALUES SHOWN IN FIRST STAGE ARE TYPICAL FOR EACH STAGE.
2. REF. DESIGNATORS ARE ABBREVIATED FOR COMPLETE NO. PREFIX DESIGNATOR WITH ASSY. NO. A4A2
3. PLUG DESIGNATOR P1
4. REF. P.C. BOARD NO 352
5. UNLESS OTHERWISE SPECIFIED, DIODES ARE IN4009, CAPACITORS ARE IN PICOFARADS. RESISTORS ARE 6.8K 1/4 WATT ±10 %
6. REF. ASSY. DC 913

Figure B6-3. 7-Stage Ring Counter Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2



NOTES:

1. COMPONENT VALUES SHOWN IN FIRST STAGE ARE TYPICAL FOR EACH STAGE.
2. REF. DESIGNATORS ARE ABBREVIATED FOR COMPLETE NO. PREFIX DESIGNATOR WITH ASSY. NO. A4A4
3. PLUG DESIGNATOR IS P1
4. REF. P.C. BOARD NO 354
5. UNLESS OTHERWISE SPECIFIED, DIODES ARE IN4009, CAPACITORS ARE IN PICOFARADS, RESISTORS ARE 6.8K 1/4 WATT ± 10%
6. REF. ASSY. D0912

Figure B6-4. 11-Stage Ring Counter Schematic Diagram

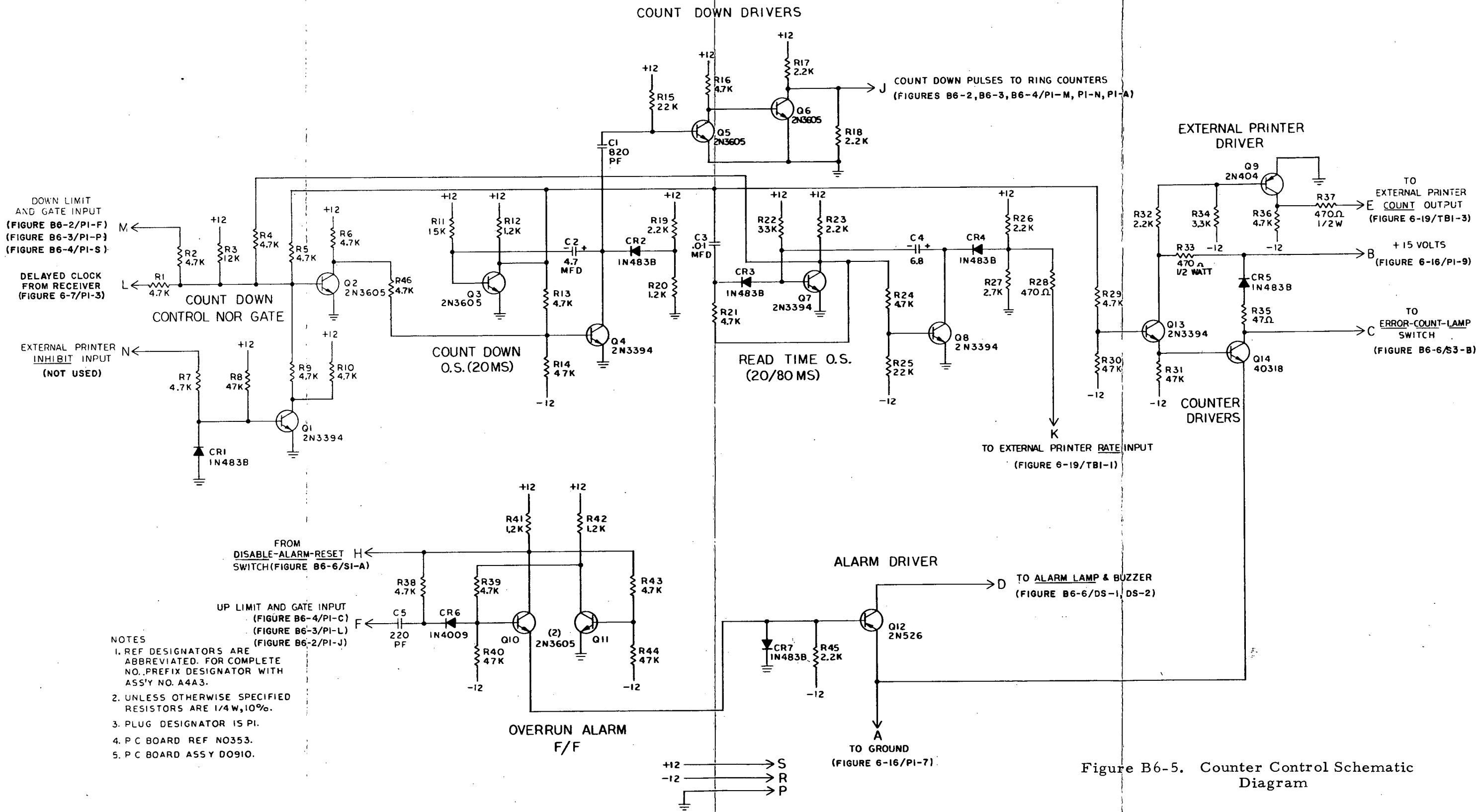


Figure B6-5. Counter Control Schematic Diagram

FOLDOUT FRAME 1

FOLDOUT FRAME 2

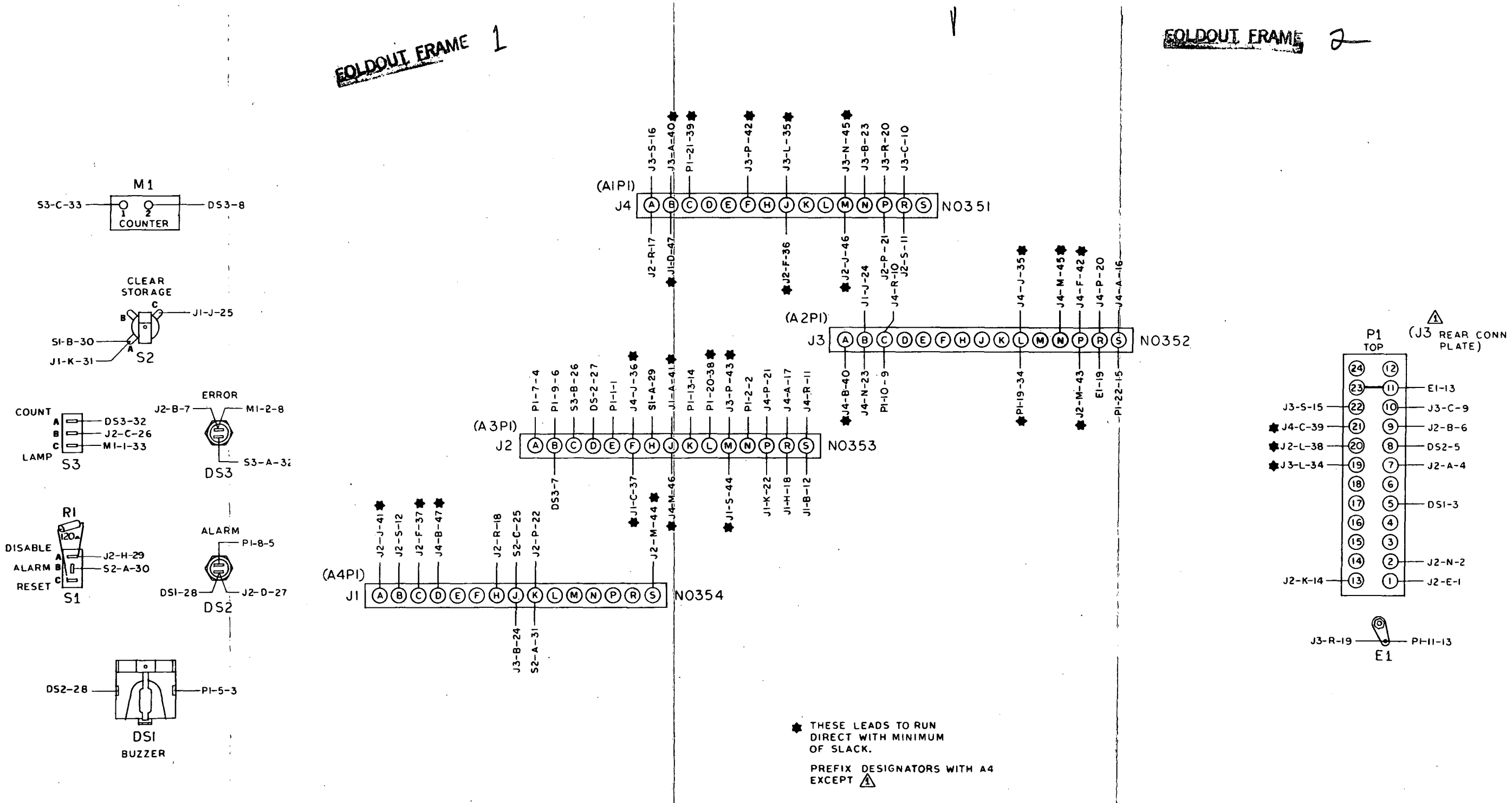
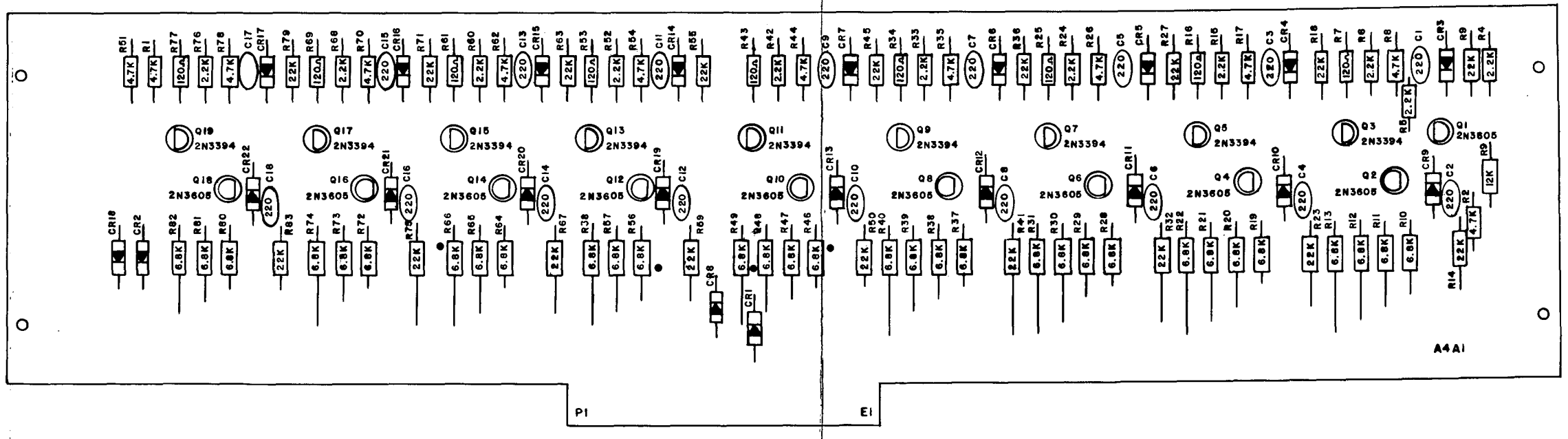


Figure B6-6. Model 600 Error Counter Module Wiring Diagram

FOLDOUT FRAME 1

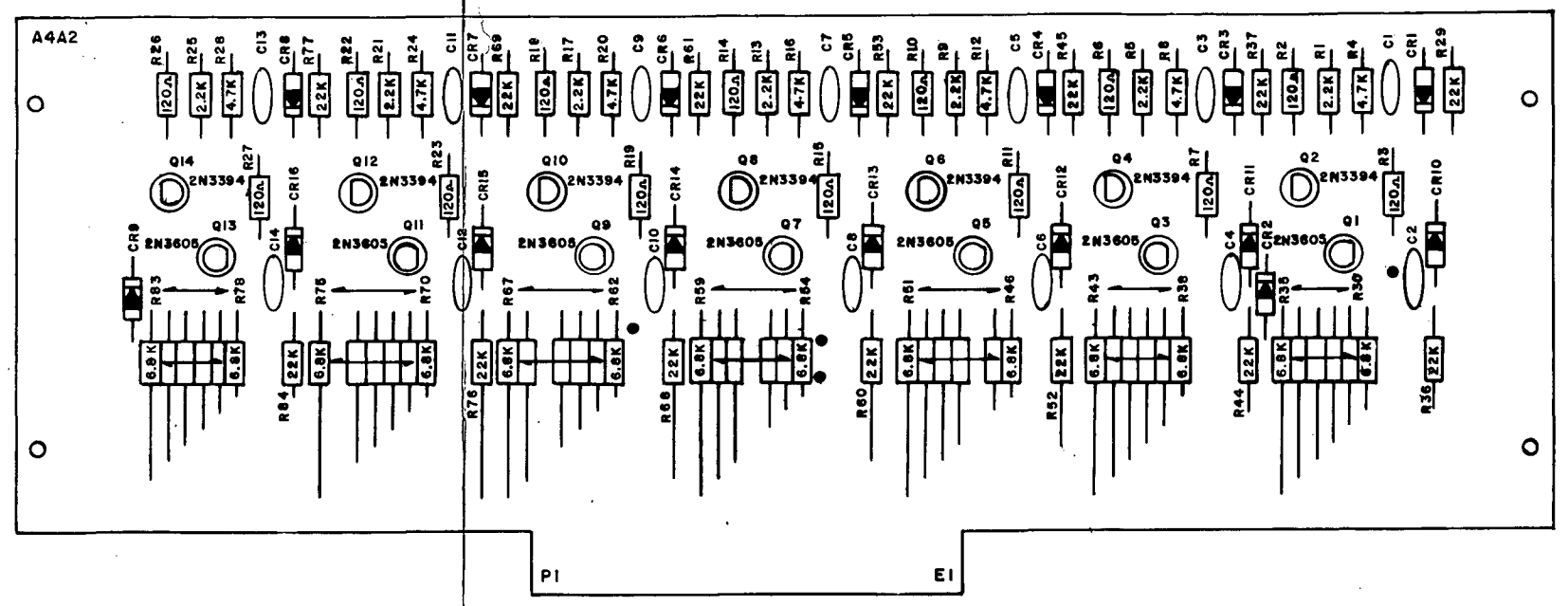
FOLDOUT FRAME 2



NOTES

1. REFERENCE DESIGNATORS ARE ABBREVIATED FOR COMPLETE NUMBER PREFIX DESIGNATOR WITH ASSEMBLY NO. A4A1.
2. REFERENCE SCHEMATIC D0915.

Figure B6-7. 4- and 5-Stage Ring Counters Assembly Diagram



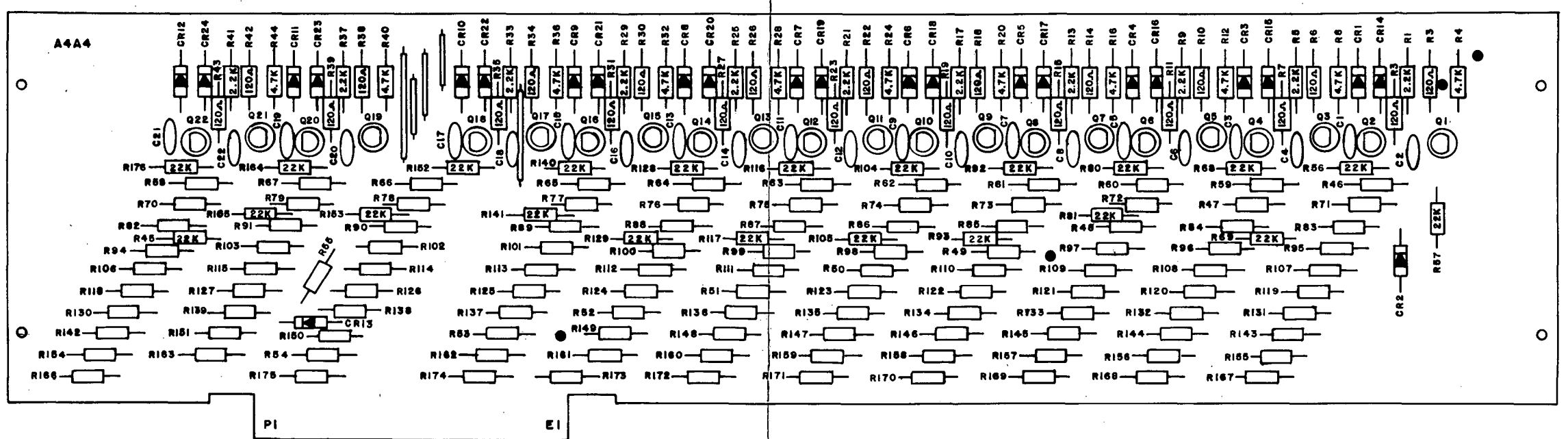
NOTES:

1. REFERENCE DESIGNATORS ARE ABBREVIATED. FOR COMPLETE NUMBER PREFIX DESIGNATOR WITH ASSEMBLY NUMBER A4A2.
2. SCHEMATIC REF: C1049.

Figure B6-8. 7-Stage Ring Counter Assembly Diagram

FOLDOUT FRAME 1

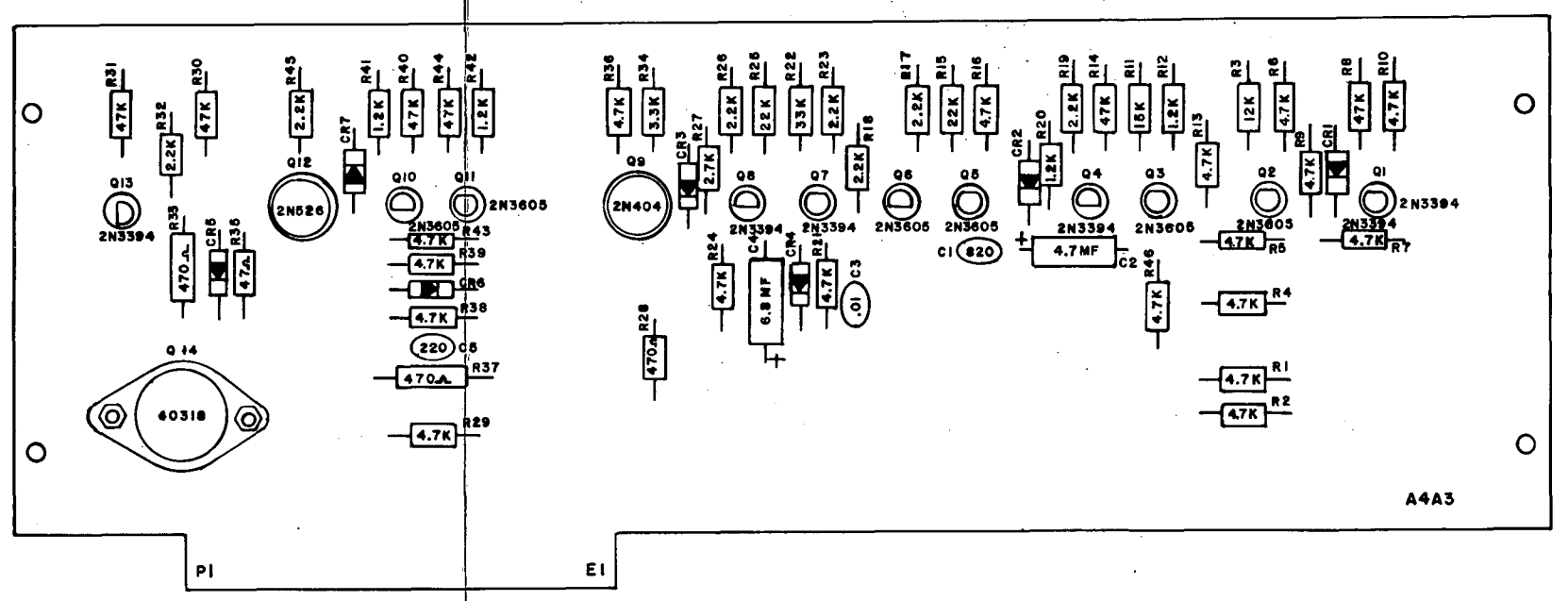
FOLDOUT FRAME 2



NOTES

1. REFERENCE DESIGNATORS ARE ABBREVIATED. FOR COMPLETE NUMBER PREFIX DESIGNATOR WITH ASSEMBLY NUMBER A4A4.
2. SCHEMATIC REF: D0909.
3. UNLESS OTHERWISE SPECIFIED RESISTORS ARE 6.8K.

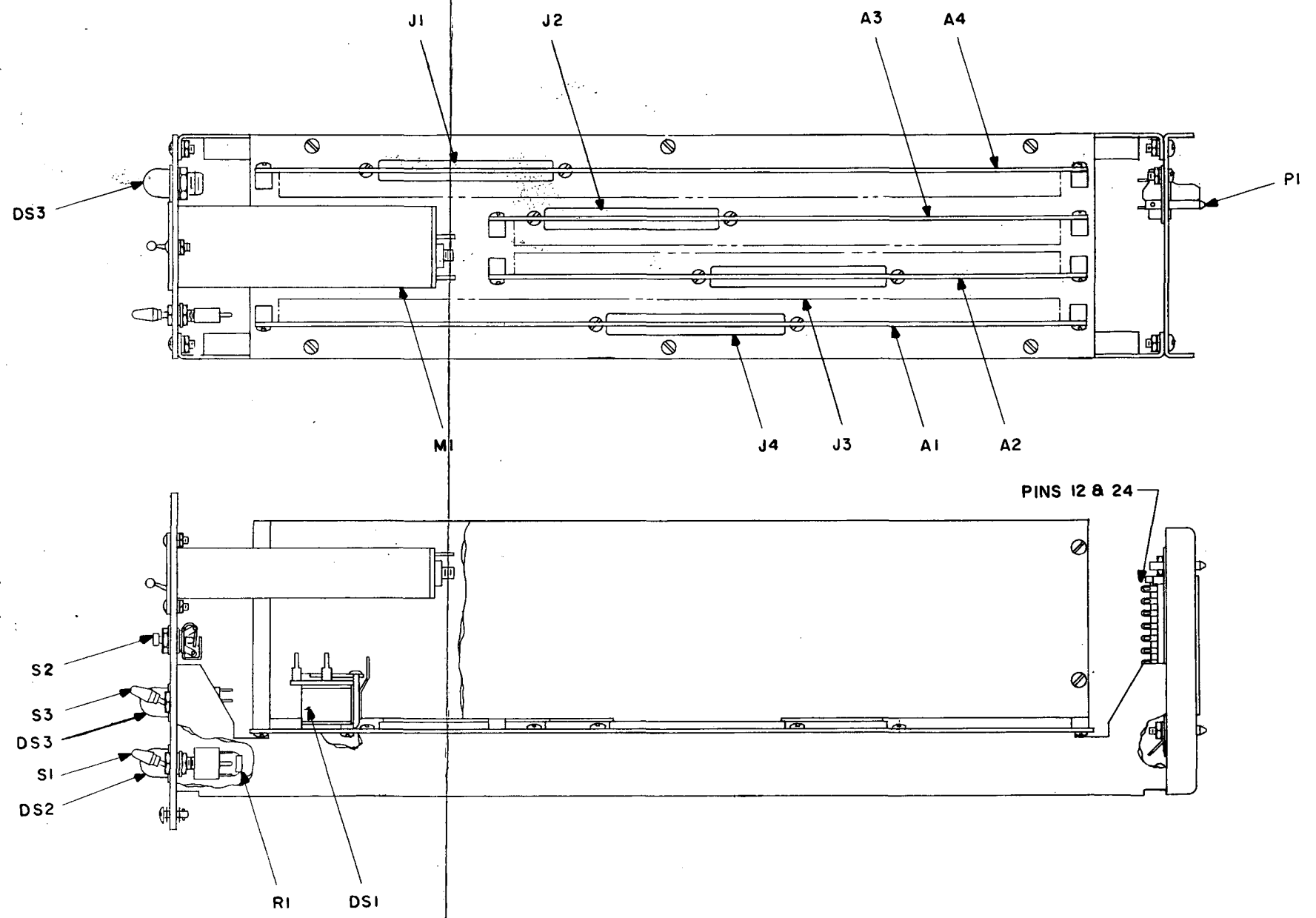
Figure B6-9. 11-Stage Ring Counter Assembly Diagram



NOTES:

1. REFERENCE DESIGNATORS ARE ABBREVIATED FOR COMPLETE NUMBER PREFIX DESIGNATOR WITH ASSEMBLY NO. A4A3.
2. REFERENCE SCHEMATIC D0911.

Figure B6-10. Counter Control Assembly Diagram



NOTES
1. WIRING DIAGRAM REF.: D0918.
2. ASSEMBLY DESIGNATOR IS A4.

Figure B6-11. Model 600 Error Counter Module Assembly Diagram

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